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Conception et Optimisation de la Tête Haute Fréquence d'un Récepteur Hétérodyne à 1.2 THz pour l'Instrument JUICE-SWI

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Résumé en Français :

La conception, fabrication et caractérisation d'un récepteur hétérodyne à 1.2 THz a été effectuée par le *Laboratoire d'Etudes du Rayonnement et de la Matière en Astrophysique et Atmosphères* (LERMA) et constitue la base de ce rapport de thèse. Les études, analyse et résultats présentés dans ce manuscrit ont été effectués dans le cadre la mission JUpiter ICe moon Explorer (JUICE). JUICE est la première des grandes missions proposées à l'agenda du programme spatial Cosmic Vision 2015-2025 de l'Agence Spatial Européenne (ESA). La mission satellitaire JUICE est consacrée à l'étude du système Jovien. La charge utile du satellite est composée de 10 instruments à l'état-de-l'art et d'une expérience. Le développement du récepteur hétérodyne à 1.2 THz présenté dans cette thèse est dédié à SWI, acronyme anglais de "Submillimeter Wave Instrument", qui, grâce à une résolution spectrale de 10^7, étudiera à partir de 2030 la structure, la composition et la dynamique des températures de la stratosphère et de la troposphère de Jupiter ainsi que les exosphères et les surfaces des lunes glacées.

La partie haute fréquence du récepteur est complètement basée sur la technologie de diodes Schottky planaires sur membrane d'arséniure de galium (GaAs), appelées "Planar Schottky Barrier Diodes" (PSBDs) dans le manuscrit. La réalisation du canal à 1.2 THz de SWI basé sur la technologie Schottky et entièrement développé par le consortium européen, dont fait parti le LERMA, a été le défi le plus significatif rencontré par ce dernier. L'extrême réduction de la taille des anodes des diodes Schottky nécessaire pour monter aux fréquences du THz a été atteinte en collaboration avec le *Laboratoire de Photonique et de Nanostructures* (LPN) en utilisant la lithographie électronique pour la fabrication de véritables "Monolithic Microwave Integrated Circuits" (MMIC).

Une partie importante du ce rapport de thèse et consacrée à l'étude des phénomènes physiques additionnels qui apparaissent quand les dimensions des diodes sont fortement réduites. En particulier, les modifications du comportement résistif et capacitif des diodes Schottky dues à des phénomènes microscopiques bidimensionnels ont été étudiées au moyen d'un simulateur bidimensionnel Monte Carlo (2D-MC), en collaboration avec l'Université de Salamanca, en Espagne.

Comme détaillé dans ce manuscrit, la caractérisation précise du comportement capacitif de la diode Schottky est un point critique pour déterminer la plage de fréquences de leur utilisation pour une application donnée. Toute modélisation imprécise de cette propriété de la diode peut entrainer un décalage significatif de la plage de fréquences d'opération d'un circuit THz.

Cependant, la modélisation précise des diodes Schottky à ultra-hautes fréquences, n'est qu'une des étapes requises pour réussir à concevoir correctement un circuit THz. L'analyse précise et méticuleuse de l'interaction entre le comportement électromagnétique du chip MMIC et le comportement physique des diodes Schottky a été le but le plus important poursuit dans ce travail doctoral pour le développement du récepteur à 1.2 THz. Cette tâche a été abordée en utilisant les outils commerciaux "High Frequency Simulation/Structure Software" (Ansys-HFSS) et "Keysight Advance Design System" (Keysight-ADS). La combinaison des simulations électromagnétiques des structures tridimensionnelles du chip MMIC (Ansys-HFSS) et les simulations du comportement électrique non-linéaire de la diode

Schottky (Keysight-ADS) est la manière actuelle d'aborder la conception de ce type de circuits THz. Le modèle électrique analytique de la diode requis par l'outil ADS a été défini par l'auteur conformément aux résultats précédemment obtenus avec le simulateur physique Monte Carlo. L'implémentation du modèle étendu de la diode Schottky dans cette méthode pour la conception et l'optimisation de chaque étage du récepteur à 1.2THz, est le sujet développé dans ce rapport de thèse. L'interaction entre le modèle physique de la diode et le modèle électromagnétique de la structure du chip MMIC est étudiée dans les diffèrent chapitres de ce manuscrit. Pour conclure, l'aspect génie-mécanique lié à ces applications THz est abordé dans la discussion. Malgré les améliorations dans les techniques de fabrication pour réaliser des structures électroniques micrométriques ou même nanométriques, la performance du récepteur à 1.2 THz dépend fortement du procédé de réalisation micro-mécanique des structures en guides d'onde et des procédures d'assemblage des composants dans ces dernières. La technique de lithographie électronique pour la fabrication des MMIC THz permet une haute reproductibilité des composants, avec une précision inférieure à 1 µm. Néanmoins, il existe encore the variations dans les propriétés physiques des diodes intégrées dans les différents composants MMIC, et ces variations peuvent être notamment marquées quand l'épaisseur de la couche d'épitaxie et la taille des anodes sont fortement réduites. Par ailleurs, la précision du procès d'assemblage des chips dépend de la précision dans les dimensions du bloc mécanique. Ces défis techniques entrainent de déviations de quelques micromètres à quelques dizaines de micromètres entre les différents modules développés, ce qui peut entrainer des dégradations importantes du fonctionnement des circuits. La prise en compte de ces défauts mécaniques dans la conception du récepteur à 1.2 THz a été aussi importante que la modélisation précise du comportement électrique et électromagnétique des composants MMIC. Plusieurs sections de ce rapport de thèse ont été dédiées à l'analyse théorique de l'impact des déviations expérimentales et la réconciliation entre les résultats expérimentaux et théoriques.

Mots clés : [Planar Schottky Barrier Diodes, frequency mixer design, frequency doubler design, heterodyne receiver, Monte Carlo]

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Acronyms

2D-MC Two-Dimensional Monte Carlo.

ADS Advance Design System.

DSB Double Side Band.

ESA European Space Agency.

ESEP Exploration Spatiale des Invironnements Planétaires.

EU Electronic Unit.

HB Harmonic Balance.

HBT Heterojunction Bipolar Transistor.

HBV Heterostructure Barrier Varactors.

HEB Hot-Electron Bolometers

HEMT High Electron Mobility Transistor.

HFSS High Frequency Electromagnetic Field Simulator.

IF Intermediate Frequency.

IR Infra-Red.

LEC Lumped Elements Circuit.

LNA Low Noise Amplifier.

LO Local Oscillator.

MC Monte Carlo.

MMIC Monolithic Microwave Integrated Circuit.

MPS Max Planck Institute für Sonnensystemforschung.

PSBD Planar Schottky Barrier Diode.

QCL Quantum Cascade Laser.

RAU RAdiator Unit.

RF Radio Frequency.

RPG Radiometer Physics GmHb.

RTD Resonant Tunneling Diodes.

RU Receiver Unit.

SIS Superconductor-Isolator-Superconductor.

SDD Symbolically Defined Device.

SSB Single Side Band.

SSEC Small Signal Equivalent Circuir.

STD STanDard.

SWI Submillimeter Wave Instrument.

THz Terahertz.

TRU Telescope and Receiver Unit.

USO Ultra Stable Oscillator.

VDI Virginia Diodes Inc.

Introduction

Abstract- The design, fabrication and testing of a frequency heterodyne receiver at 1.2 THz has been developed by *Laboratoire d'Etudes du Rayonnement et de la Matière en Astrophysique et Atmosphères* (LERMA) and it is the foundation of this dissertation. The studies, analysis and results presented in this manuscript have been carried out within the framework of the JUpiter ICe moon Explorer (JUICE) mission. JUICE is one of the proposed missions in the agenda of the European Space Agency (ESA) Cosmic Vision 2015-2025 program. The objective of the JUICE satellite mission is to study the Jovian system, especially the Jupiter atmosphere properties and the surface characteristics of its icy moons. Scientific equipment consisting of ten state-of-the-art instruments and one experiment comprise the payload of this satellite. The development of a 1.2 THz channel is part of the Submillimeter Wave Instrument (SWI) devoted to recovering the spectroscopy data of the Jupiter atmosphere and icy-moons' surface composition. The scientific principle for this receiver is all-solid-state semiconductor technology based in GaAs Planar Schottky Barrier Diodes (PSBDs). The achievement of a 1.2 THz channel based in PSBDs totally developed by European partners was the major challenge proposed for SWI, with LERMA committed to this assignment. The required ultra-scaling of the Schottky anode size of PSBDs in the attainment of the THz range has been achieved in collaboration with *Laboratoire de Photonique et de Nanostructures* (LPN) using e-beam photolithography in the fabrication of Monolithic Microwave Integrated Circuits (MMIC). An important part of this dissertation addresses the appearance of additional physical phenomena when ultrascaling solid-state PSBDs. Particularly, the modification of the electrical resistivity and capacitance of SBDs due to two-dimensional phenomena has been studied by means of a physical microscopic Two-Dimensional Monte Carlo (2D-MC) simulator, in collaboration with the University of Salamanca, Salamanca, Spain. As discussed within this manuscript, the accurate characterization of the diode capacitance is one of the critical points when opening a frequency window in the required frequency range of a THz application. A misunderstanding of this modified capacitance during the design of these devices can lead to a considerable offset in the frequency range of the experimental module. However, the accurate modeling of PSBDs in such high frequency applications is only a part of the expertise required for the successful completion of this challenge. The accurate and meticulous analysis of the

interrelationship between the electromagnetic behavior of the MMIC chip and the physical behavior of the integrated PSBDs is the main challenge faced in this dissertation for the development of the 1.2 THz receiver. This task has been addressed using the commercial Ansys High Frequency Simulation/Structure Software (Ansys-HFSS) and the Keysight Advance Design System (Keysight-ADS). The combination of the three-dimensional electromagnetic characterization of the chip structure (obtained with HFSS) with the non-linear electrical circuit simulation (carried out by ADS) of diodes is the current methodology for the design of these modules. The analytical electrical model of PSBDs required by ADS software has been defined by this author in agreement with the results obtained with the 2D-MC simulator. The implementation of this approach in the design and optimization of the different stages of the accomplished 1.2 THz receiver is the main subject of this dissertation. The interaction between the physical model of the PSBDs and the electromagnetic modeling of the structure will be discussed within the different chapters of this dissertation. Finally, the mechanical engineering of these applications must be addressed in this discussion. Although the advancements in the fabrication techniques to accurately engineer micrometric and even nanometric structures, the ultrahigh frequency pursued by SWI project makes the final performance of the receiver to depend on the precision of the assembly process. The e-beam photolithography technic for the MMIC fabrication can reach a precision level below 1 μm, allowing a high reliability of the chips. However, the final physical properties of each single diode integrated in different MMIC chips can vary between different chips, especially when reducing the epitaxial profile and anode size dimensions. Additionally, the precision of assembly process of the chips resides in the accuracy of the mechanical block dimensions, which leads the electromagnetic signals into the chip, and the positioning of the chips in the block, which is finally addressed by manual methods. These technical challenges lead to final deviations of some tens of micrometers between different units of the developed modules, which are comparable to the wavelengths of the treated signals up to 1.2 THz. The understanding of these technical facts on the design of the receiver has therefore been as critical as the accurate modeling of the electromagnetic and electric behavior of the MMIC chips. For this reason, several sections within this dissertation have been devoted to the theoretical analysis of the technical deviations faced in practice as well as the reconciliation between experimental and theoretical results.

1 The Submillimeter Range for Planetary Science

The submillimeter-wavelength range is the so-called Terahertz (THz) frequency range and it is usually associated with the electromagnetic spectrum of radiations from 1 mm of wavelength (300 GHz of frequency) to 0.03 mm of wavelength (10 THz of frequency). This frequency range has given rise to an intense scientific interest since at least the 1920s [Nich25], but the historical study of the millimeter and the submillimeter range starts in 1890s [Wilt84]. The research on THz science is far from being completed but a detailed summary of the development of this science can be found in [Sieg02]. The THz range remains an important technological challenge today. It has two important facets since the THz frequency range is difficult to reach by both electronic-based sources, when moving up from lower frequencies, and optics based sources, when moving down from upper frequencies. The present work is focused on the electronic-based devices for submillimeter applications. Very important advancements have been carried out in electronic-based devices and the THz range has spread out through diverse technological applications in which the absence of a compact high-efficiency and high-power THz sources is the common ground. The THz range is currently applied in the medical field [Tada04], [Pick06], in spectroscopy [Gopa98], [Encr04], [Shi04], [Hans07], [Luci10] and in THz imaging for multiple applications [Chan07], [Coop08], [Bryl09], [Coop14]. However, it is in atmospheric, planetary and astrophysics sciences as well where the development of THz technologies has been especially enhanced. The interest comes from the large amount of electromagnetic radiation in the THz and far Infra-Red (IR) ranges associated with observable universe that has attracted the attention of astronomers since the early stages of this science [Sieg02]. For example, the kinetic analysis of galaxy dust using the detection of high rotational transitions of the CO molecule lines which are redshifted to millimeter wavelengths [Cox02].

The spectroscopy has been especially important in the development of THz science which has also required the development of THz receivers. The detection of a frequency signal in electronic-based circuits usually consists of a preliminary stage conformed by a Radio Frequency (RF) antenna, which is able to capture a certain frequency range, an electronic device sensitive to those frequency signals and a Low Noise Amplifier (LNA). The first challenge found in THz science to develop THz receivers is the LNA since all solid-state transistors have a cutoff frequency from which the amplification capabilities of the device are dramatically degraded. The commercial THz amplification solid-state technology that has spread out during the last decades is able to rise to W-band (75 – 110 GHz) [IEEE std. 521-2002] using High Electron Mobility Transistors (HEMTS), metamorphic HEMTs (mHEMTs) and Heterojunction Bipolar Transistors (HBTs) mostly based on InP and GaAs semiconductor (SC) structures [Samo11]. Additionally, these devices allow THz amplifiers for broadband applications (bandwidth ~20 % of the center frequency) that can operate at room temperature. Commercial Monolithic Microwave Integrated Circuits (MMIC) amplifiers up to 100 GHz are commonly found up to W-band [Wang01], but higher frequency broadband amplifiers around 200 GHz [Wein99], [Deal07a], [Chio16], around 300 GHz [Deal07b], [Tess08] and even up to 600 GHz [Seo13], [Tess14], [Deal16] have already been demonstrated. A lot of narrowband amplifiers can be found even at higher frequencies using diverse technologies

[Truce14]. However, most of these amplifiers are not commercialized and the technology is carefully controlled by the manufacturers or even restricted for military applications. This leads to lower frequency amplifiers up to W-band (75 – 100 GHz) that have been commonly commercialized. The application of this technique based on GaN amplifiers is providing higher output power at W-band during the last years [Mish08], [Sile08b], [Sche16], [Marti16] and it could eventually replace the actual GaAs and InP-based W-band amplifiers in a near future. The availability of a commercial W-band LNA has also been a prior objective that has encouraged significant research [Mei08], [Brye09], [Yang13], [Pepe15], [Zhan16]. This absence of commercial availability of higher frequency amplifiers has hampered THz detection, especially in room temperature direct detection applications at THz frequencies which is nowadays limited up to W-band [Hoef14], [Deco16].

The alternative technology that has placed itself in the THz detection field due to its sensitivity and high spectral resolution (1-100 MHz) at THz frequencies is the heterodyne detection technique. The development of a 1.2 THz heterodyne receiver is the subject of this work and the different motivations that have enhanced the accomplishment of this work are pointed out in this section.

1.1 The Heterodyne Detection

The heterodyne reception is a widespread technique in most of the THz applications developed for THz science since these kinds of receivers allow moving up on frequency beyond the 1 THz RF detection [Sieg02]. A general scheme of a heterodyne receiver for THz applications is shown in Fig. 1.1. A THz heterodyne electronic-based receiver requires a Radio Frequency (RF) mixer module sensitive to certain THz frequency ranges coming from a RF source. This mixer module needs to be pumped by a THz power source, so-called Local Oscillator (LO), able to yield a very precise frequency signal under W-band (with only some few tens of MHz wideband) that is then multiplied *N* times to increase the frequency up to the mixer requirement. A telescope and optical bench are usually used to increase the effective detection surface and focus the signal into the RF horn of the mixer. The RF signal at frequency f_{RF} is mixed with the LO signal at frequency f_{LO} by the mixing stage resulting in an Intermediate Frequency (IF) signal at frequency $f_{IF} = f_{RF} - n \cdot f_{LO}$, where n refers to the n-th harmonic of the LO frequency signal [Hayk08]. It is possible to differentiate between fundamental heterodyne receivers if $n = 1$ and sub-harmonic receivers if $n \geq 2$. The heterodyne receiver developed in this work corresponds with the second kind with n = 2. These receivers are usually designed to generate an IF signal low enough to be amplified by commercial LNAs, i.e., the considered frequency of the LO signal (or its *n*-th harmonic) is similar to the detected RF frequency signal. Usually, no LNA is used in THz heterodyne receivers to amplify the captured RF signal by the RF antenna since there isn't frequency LNAs able to efficiently work beyond W-band. This result in a LO input power which is usually much higher than the RF input power in these receivers. The principles of frequency mixing using non-linear devices can be found in [Man56], [Pant58], [Ebst67], [Sea69].

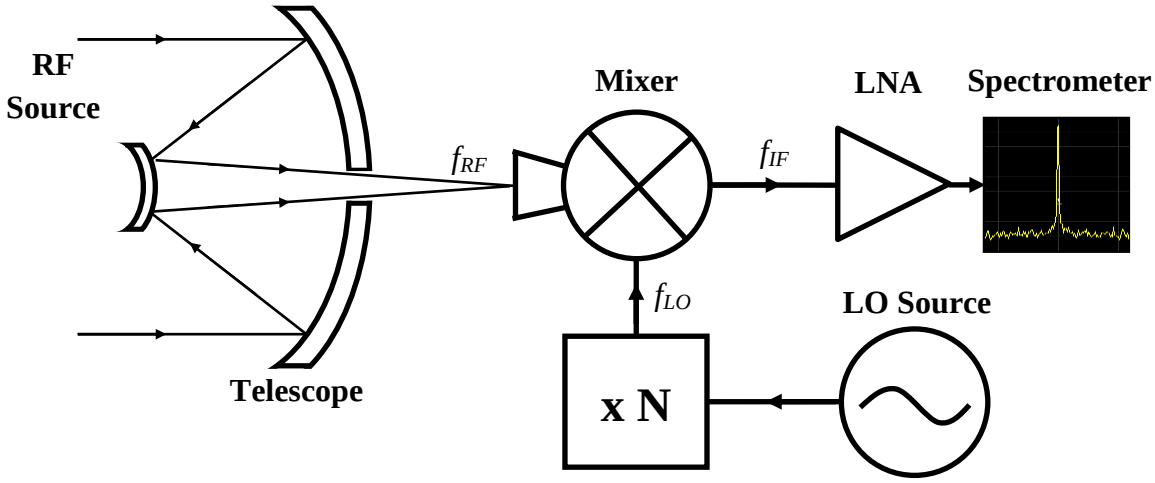

Fig. 1.1. Scheme of a heterodyne receiver for THz detection.

In conclusion, the heterodyne reception avoids the necessity of LNA beyond W-band but obtaining a THz source for the LO and an adequate device for the mixing stage are the challenges presented by these receivers.

1.1.1 THz Frequency Mixers

The most critical element of the heterodyne reception is the frequency mixer and especially the non-linear devise used to efficiently mix the LO and the RF signal. Several technologies

have been studied in THz science for mixing applications but the most widespread devices are the Superconductor-Isolator-Superconductor (SIS), the Hot-Electron Bolometers (HEB) and the Planar Schottky Diodes (PSBDs). The SIS technology has proven to be the best device for mixing applications since frequency heterodyne receivers, with Single Side Band (SSB) noise temperature as low as 2 times the quantum noise limit (*hf/k*), have been demonstrated [Kerr99], [Koll02], [Chat08], [Maes10b], [Bill13]. Additionally, these mixers can perform a broadband IF band [Laur01], [Pan04] with low LO power requirements. However, the SIS mixers require cryogenic temperatures to work and they are limited up to 1.5 THz, mainly due to the disappearance of the superconductor properties [Karp07], [West13], [Zmui15]. The HEB has been placed itself as the alternative device that is able to replace the SIS beyond its frequency limit. The HEB are also required to be cooled down to 2 - 4 K but frequency receivers up to 4.7 THz have been demonstrated with DSB noise temperatures 10-20 times the quantum noise limit [Haje04], [Chat07], [Cher08], [Tret11], [Buch15]. HEB are able to provide the best performances using very low LO input power, hundreds of nW, which is possible to obtain with both electronic and optical based THz sources. The challenge of HEBs is the short IF bandwidth that it is possible to provide and the cooling system requirement. Regarding the PSBDs technology, it can provide frequency receivers with DSB noise temperature much higher than SIS and HEB, above 50 times the quantum noise limit, but it is able to work at room temperature. This results in extremely compact frequency mixers that do not require any cryogenic system [Chat07], [Maes10b]. Additionally, the performance of PSBD mixers is always improved down to 30-40 times the quantum noise limit when cooling down below 150 K [Pred84], [Schl14], [Treu16]. Very important efforts are focused now to develop frequency mixers based on Schottky technology that will overcome the SIS frequency limit in a near future [Treu16b]. The challenge of PSBD mixers is the high LO power requirements compared with HEBs and the higher noise provided as the frequency increases. This work is focused on the development of a 1.2 THz mixer based on PSBD technology. The PSBD technology has positioned itself as the most suitable option for space-borne applications that do not require the most sensitive receivers, like planetology or remote sensing of the Earth's atmosphere, due to the compact low-weight receivers that can be achieved.

1.1.2 THz Local Oscillator

One of the most difficult challenges faced by the THz science community, which has not been addressed yet, is obtaining a powerful, efficient and compact THz source. The main challenge when reaching the THz range in electronic-based applications is associated to an electron transit time in the same order of the THz frequencies, hampering the proper functioning of electronic-based devices when moving up in frequency. Similarly, a THz laser based on an energy transition requires transition energy of the same order as the room temperature lattice vibrations in the material, hampering the proper functioning of optic-based devices when moving down in frequency. The development of electronic-based THz sources using solid-state oscillators has been pursued for several decades. One of the most promising THz oscillators above 100 GHz is based on InP Gunn devices, thoroughly studied by Dr. Carlstrom [Carl85] and Dr. Eisele in [Eise95], [Eise97], [Eise00], [Eise04], [Eise06], [Eise10] and by Dr. Khalid in [Khal07], [Khal13]. The Gunn diodes were widely used in the (sub)-

millimeter heterodyne receivers in the past. However, Gunn diodes require phase locking, are difficult to tune and to use in broadband frequency applications. Gunn oscillators have been currently replaced by amplify-multiply chains. Interesting advancements have been carried out during the last years by Tokyo Institute of Technology in fundamental THz source based on Resonant Tunneling Diodes (RTDs) up to 1.46 THz [Feig14] and 1.92 THz [Maek16]. Regarding the optical based THz source, the Quantum Cascade Laser (QCL) technology has placed itself as the leading mid-infrared (mid-IR) source since it was proposed twenty years ago and it has shown itself to be the most suitable way to substantially reduce the frequencies even down to 1 THz [Will07]. However, the challenge faced by QCL sources is avoiding the cryogenic temperatures requirement that notably hampers this technology to spread out in the THz applications [Belk15]. Other techniques use crystals as coherent THz source [Shi02]. An intermediate technique that combines optical and electronic base devices is based on photo-mixers and it allows obtaining LO power sources suitable to pump SISs or HEBs based mixers. The photo-mixers can mix two laser beams at IR range to generate an electrical signal at required LO frequencies [Font07], but this technique usually requires cooling systems due to the low conversion efficiency of the photomixers and the high amount of power dissipated in the device. Low LO power sources can be provided by this technique.

The alternative electronic-based technology that has been able to place itself in the commercial applications at THz frequencies is based on frequency multiplication. The technique used in this work, which is able to provide the highest LO power electronic-based sources know nowadays, consists of a preliminary commercial Ultra Stable Oscillator (USO), at a single frequency of few tens or hundreds of MHz [Cand03], followed by a commercial Frequency Synthesizer [Tobi01] that is able to generate a broadband frequency window up to some tens of GHz [Jain09] using the reference given by the USO. The generated millimeter wavelength source can be amplified using available commercial amplifiers obtaining some hundreds of mW at E-band (60-90 GHz) and multiplied to move beyond 100 GHz. The multiplication chains usually consist of an assembly of frequency doublers and triplers in accordance with the desired output frequency signal and the available amplifier source [Sieg02]. It is based on the excitation, at a specific frequency f_1, of a passive non-linear solid-state device whose response will contain the fundamental frequency f_1 and its harmonics $n\ f_1$ with n= 2, 3,…, ∞. Electronic-based frequency doublers and triplers usually consist of a waveguide system to lead the input and output frequency signals and a passive non-linear solid-state device mounted in a microelectronic chip. The microelectronic chip is designed to couple the input signal in a certain frequency and power range and it also couples the desired frequency harmonic generated by the non-linear device with the output waveguide system. The most important electronics-based device technologies used currently in the THz multiplication field are the Heterostructure Barrier Varactors (HBVs) and the PSBDs previously mentioned.

The LO source used in this work is also based on the second type of devices, i.e., the 1.2 THz receiver developed in this work is an all-solid state PSBD heterodyne receiver. The theoretical foundation of the so-called metal-semiconductor rectifiers started in 1931 when the band model of SCs was formulated [Wils31]. The fundaments of Schottky barrier diodes were proposed by W. Schottky in 1938 [Scho38] and H. A. Bethe formulated in 1942 [Beth42] the

well-known thermionic emission theory that describes the electrons transport through the Schottky barriers. The HBVs were first introduced by Kollberg and Rydberg in [Koll89], [Rybd90] and they can only be used in odd harmonic multiplication due to the internal symmetry of the device. HBVs are suitable for frequency triplers [Salg03], [Vuku12] and especially useful in quintupler applications providing efficiencies higher than PSBDs [Bryl12], [Malk15]. Nevertheless, it is the Schottky technology which is widespread in millimeter and submillimeter applications, especially for ground-base and space-borne heterodyne applications since it is able to provide the highest efficiencies, output power and instantaneous bandwidth [Maes05a]. It is mainly because PSBDs can be used in different configurations to design both doublers and triplers as varactor mode, and it can also be used for mixing applications in varistor mode. It can work at room temperature, allowing PSBD based modules to be very compact and robust. They can easily pump frequency mixers based on HEB or SIS technologies. It has motivated the development of a wide range of PSBDs frequency broadband multipliers since the 1990s from 100 GHz to up to 2.7 THz [Eric93], [Schl01a], [Maes05a], [Maes06], [Maes08], [Maes10a], [Sile11a], [Maes12], [Treu14], [Sile15]. Different combinations of doublers and triplers in a multiplication chain based on PSBDs also allow the development of THz sources at different frequency ranges using the same millimeter source. A summary of the actual THz electronic and optic-based sources availability can be found in [Maes10b (Fig.1)] and [Will07], respectively.

1.1.3 Space missions and THz science

Some of the most important space missions where a millimeter or submillimeter instrument was proposed are summarized in this section. The common ground between these mission is the implementation of some of the different technological approaches used to define the technical specification of the SWI instrument. The development and implementation of these space missions summarized the background that has motivated the basis of JUICE-SWI project and this work.

A. *Ground-based millimeter and Sub-Millimeter Telescopes*

The ALMA project [ALMA 2016] is the largest ground-based radio-telescope currently existing for millimeter and submillimeter astronomy interferometry and it is placed in the Atacama Desert, Chile. It consists of 54 antennas of 12 m diameter equipped with frequency receivers based on SIS mixers covering the 30-950 GHz [Brow04]. ALMA has operated since 2009 but it was inaugurated in 2013. ALMAs receivers are based on SIS mixers and the LO chain is mainly based on MMIC Schottky diodes multipliers [Brye05], [Morg05] that were developed by VDI. The W-band power amplifiers drivers are based on MMIC InP HEMTs technology [Samo05]. ALMA was develop to improve the performances and complement the already existing submillimeter telescopes such as the James Clerk Maxwell Telescope (JCMT) in Hawaii and interferometers as the Institut de Radio Astronomie Millimétrique (IRAM) in France. The JCMT [Murd00] is placed in Hawaii island and it is a single 15 m diameter dish dedicated to the detection of submillimeter radiation between 1.4 to 0.4 mm wavelengths. The IRAM [Maar87] was established in 1984 in Pico Veleta, Spain, and it is a 30-m millimeter radiotelescope. It had

a complementary array of three 15-m antennas placed on Plateau de Bure Observatory, France, which has eventually been extended to six antennas and finally replaced by the current NOEMA project since 2014 with six additional 15-m antennas. The six array NOEMA project is expected to be completed in 2019, becoming the most powerful millimiter radiotelescope in the North Hemisphere [IRAM-2016].

B. *Earth Observing System: AURA Satellite*

The AURA satellite was launched on July 2004 as part of the NASA's Earth Observing System (EOS) program. This science program is dedicated to monitoring the complex interactions that affect the globe. The AURA satellite is in a sun-synchronous orbit specifically dedicated to analyzing climate change by monitoring the interactions of the ozone and other chemical compounds with the radiation. AURA consists of four instruments dedicated to the analysis of the ozone and other greenhouse compounds from different aspects. The High Resolution Dynamics Limb Sounder (HRDLS) is dedicated to analyzing infrared emission, the Microwave Limb Sounder (MLS) to analyzing microwave emission, the Tropospheric Emission Spectrometer (TES) and the Ozone Monitoring Instrument (OMI).

The MLS instrument [Wate06] was one of the first important microwave space-borne instruments that enhanced the development of this technic. It is an on-board submillimeter instrument based in heterodyne reception in broad spectral regions centered at 118, 190, 240 and 640 GHz and 2.5 THz. All solid state technology was used for the local oscillators, excepting in the 2.5 THz, and MMIC amplifiers for the 118 GHz channel. All the frequency mixers were based in planar technology [Sieg93].

C. Microwave Instrument for Rosetta Orbiter (MIRO)

The Rosetta mission is a comet mission accepted by the ESA in November 1993 in the framework of the long-term program "Horizon 2000" [Glas07]. It consists of two mission elements, the ROSETTA orbiter and the PHILAE lander. ROSETTA was launched in March 2004 featuring the unprecedented assembly of 25 payload-experiments. The main scientific objectives of ROSETTA were the study of the origin of the solar system by studying comets. ROSETTA took contact with the comet 67P/Churyumov-Gerasimenko in summer 2014 and PHILAE lander was successfully deployed at the end of 2014. The mission was a complete success and it finished in September 2016 [ROSETTA-Mission-2016]. One of the ROSETTA instruments is the so-called Microwave Instrument for Rosetta Orbiter (MIRO). A precise description of MIRO and the molecules studied by it can be found in [Gulk07]. This is a heterodyne spectrometer working at two frequency ranges around 190 GHz and 562 GHz. The frequency mixer modules of MIRO are based on PSBD technology while the LO multiplication chain is a combination of different technologies. The LO source is based on InP Gunn devices to generate a LO signal around 95 GHz. This Gunn source is enough to directly pump the PSBD-based sub-harmonic mixer for the 190 GHz channel of MIRO, while a HBV-based frequency tripler is used to increase the frequency of the signal to pump the PSBD-based sub-harmonic mixer of the 562 GHz channel. This heterodyne receiver didn't require any cooling system and it has

successfully demonstrated the PSBD technology capabilities as mixer stage for space-borne front-end heterodyne detection.

D. HESHEL Space Observatory

The development of THz science has been especially encouraged by the atmospheric, planetary and astrophysics sciences which have enhanced and positioned the different available THz technologies as actual state-of-the-art. One of the first space missions that has enhanced the development of the heterodyne reception is the Far Infra-Red and Submillimeter Telescope (FIRST) mission led by the European Space Agency (ESA) in the "Horizon 2000" science plan. This telescope was expected to be put in a geostationary Earth orbit in late 2005 and featuring a payload of two instruments and at least 3 m telescope mirror [Pilb97]. The launch was delayed and the project was renamed as "HERSHEL", in honor of Sir William Hershel who discovered the Infra-Red spectrum. The HERSHEL space observatory was finally launch in 2009 and it was the largest infra-red telescope launched until the mission ended in 2013. HERSHEL finally featured a 3.5 m telescope mirror and three instruments, the Photodectective Array Camera and Spectrometer (PACS), the Spectral and Photometric Imaging REceiver (SPIRE) and the Heterodyne Instrument of Far Infra-red (HIFI) [Pilb10]. It was the HIFI instrument which motivated an intense activity in THz heterodyne technology based on multiplication and mixing stages up to the desired frequency channels. HIFI is a set of 7 heterodyne receivers that are electronically tunable, covering a 0.48-1.25 THz range in five bands using SIS mixers and a 1.41-1.91 THz range in two bands using HEB mixers. A cryostat was included in the payload module of HERSHEL due to the cryogenic requirements of these technologies. *Laboratoire d'Etudes du Rayonnement et de la Matière en Astrophysique et Atmosphères* (LERMA) was involved in the development of the SIS mixer used in the first band between 480-640 GHz. The main interest of these frequency ranges was focused on water lines analysis, surveying the molecular complexity of the universe and observations of ionized carbon for redshift analysis. Each receiver had two LO multiplier chains completely based on planar Schottky diodes technology with their corresponding W-band amplifiers [Samo00]. The LO chain for each receiver development was strongly enhanced by JPL and some details can be found in [Pear00], [Pear03], [Maes06a]. The complete development of the LO chain based on Schottky diodes technology not only allowed high-power handling capability and an improved reliability and stability of the receivers, but it dramatically reduced the cryogenic system requirements of HIFI. Nevertheless, HERSHEL was operational during 3.5 years due to the limited cryogenic gas stock.

The success of HERSHEL-HIFI, together with ROSETTA-MIRO, has laid the basis of the space-borne THz science, where Schottky technology has demonstrated an important role. The progress made during the last two decades in the completion of such important scientific goals and the developed techniques have motivated a wide range of future space mission proposals. JUICE mission was elected in the framework of the ESAs "Cosmic Vision 2015-2025" program [ESA-Cosmic-Vision (2016)]. This work is focused on the development of a part of the sub-millimeter instrument of JUICE as described below.

1.2 The JUICE Project Baseline

The Jupiter Icy Moons Explorer (JUICE) is the first large class mission chosen in the framework of the Cosmic Vision 2015-2025 program of the Science and Robotic Exploration Directorate of the ESA. The mission has been chosen in May 2012 out of three possible L-class missions in the Cosmic Vision 2015-2025 program [Doug12]. A detailed description of the JUICE mission science goals and perspectives can be found in [Gass13]. The JUICE spacecraft is expected to be launched in 2022 and reach the Jovian system eight years later, where it will perform a three year minimum-tour investigating the atmosphere and magnetosphere of the giant. The JUICE mission will survey the Jovian system with a special focus on the three Galilean Moons; Europa, Ganymede and Callisto, It will be the first spacecraft ever to orbit a Moon (Ganymede) of a giant planet. The main science goal of JUICE is *"the emergence of habitable worlds around gas giants"* by studying the presence of necessary conditions to sustain life in current habitats of the Solar System [Doug12]. The devoted science payload of JUICE consists of 10 state-of-the-art instruments and one experiment which uses the spacecraft telecommunication system with ground-based radio telescopes. The different instruments proposed in the JUICE mission baseline are listed below and a detailed analysis of the science goals pursued by each one can be found in [Gass14] and [Plau14]:

- Gravity & Geophysics of Jupiter and Galilean Moons (3GM) to study the moon gravity fields.
- Ganymede Laser Altimeter (GALA) to study moon surface topography.
- Jovis, Amorum ac Natorum Unique Scrutator (JANUS) to study the geology and surface processes in the visible range.
- Magnetometer for JUICE (J-MAG) to study moon and Jupiter magnetic fields.
- Moons And Jupiter Imaging Spectrometer (MAJIS) to study the composition of moon surfaces and Jupiter atmosphere in the visible-IR range.
- Particle Environment Package (PEP) to study plasma particles.
- Planetary Radio Interferometer & Doppler Experiment (PRIDE) is the experiment that uses a ground-based Very-Long-Baseline Interferometry (VLBI) to provide precise determination of the moons ephemerides.
- Radar for Icy Moon Exploration (RIME) to study moon-subsurface ice shells and shallow liquid water.
- Radio & Plasma Wave Investigation (RPWI) to study the radio emission and plasma of Jupiter and moons.
- Sub-millimeter Wave Instrument (SWI) to do spectrometry of Jupiter atmosphere and the moon surfaces and exospheres.
- UV imaging Spectrograph (UVS) to study moon exospheres and Jupiter auroras.

The ensemble of these instruments comprises the science payload of the JUICE spacecraft. The instrument that has motivated the present work is the SWI instrument and it will be the most important submillimeter science space-borne instrument after HIFI.

1.2.1 The Submillimeter Wave Instrument (SWI)

JUICE-SWI is a submillimeter heterodyne spectrometer with a frequency resolution of ~10^7 covering two spectral ranges around 600 GHz and 1200 GHz [JUICE-SWI-Payload (2016)] proposed by an European international consortium headed by the Max Planck Institute für Sonnensystemforschung (MPS) of Gottingen, Germany [Hart13]. The science objectives of SWI are the investigation of the middle atmosphere of Jupiter and the atmospheres and exospheres of the Galilean satellites [Hart13]. SWI consist of three primary units: the Telescope and Receiver Unit (TRU), the Radiator Unit (RAU) and the Electronic Unit (EU).

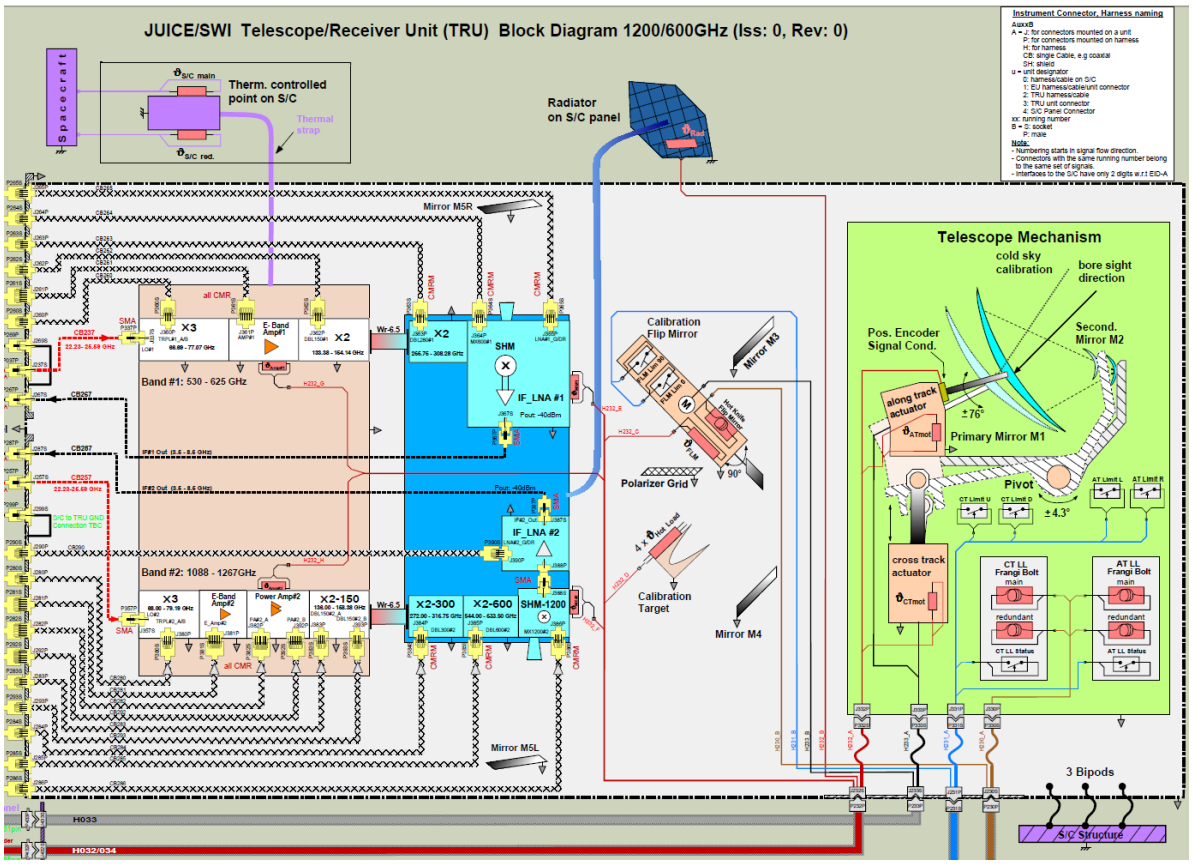

Fig. 1.2. JUICE-SWI RTU block diagram of the different parts of the instrument, as 21th June 2016. The Receiver Unit (RU) in light blue is the only cooled part of the SWI instrument.

- The RTU consists of the Telescope Unit (TU) with a 30 cm antenna effective diameter with tracking mechanisms and a receiver optical bench, and the microelectronic modules of the sub-millimeter Receiver Unit (RU). Two independent double sideband receivers were initially proposed in the SWI baseline to obtain simultaneous observing capability for two different frequencies within the 530-625 GHz frequency range [Jaco15]. However, an alternative configuration was open in the baseline of the submillimeter instrument shown in Fig. 1.2. It consists of two independent double sideband receivers, around 600 GHz and 1200 GHz. This optional second channel was never developed based on PSBDs in Europe and the only precedent was developed by JPL in the USA [Schl14]. The 1.2 THz channel was motivated by methane transition at 1256 GHz but a wide richness of compounds can be found in this frequency range [Encr04]. However, this channel had to be demonstrated and developed by the European SWI consortium in

order to be included in the fly RTU module. LERMA got involved in the development and demonstration of the 1.2 THz channel for SWI which is the motivation of this PhD. work.

- The RAU consists of a radiator used to passively cool down the Sub-millimeter detectors between 120-150 K to improve their sensitivity and their signal-to-noise ratio.
- The EU consists of several electronic devices dedicated to determine the spectral line shapes and the lines surveys. A detailed study of the SWI structural and tracking systems of the RTU is carried out in [Jaya14].

The different contributions of European institutions in the consortium were distributed as follows. LERMA represents the French contribution distributed between the RU and the EU. MPS represents the German contribution to the structure design and manufacture of the RTU and RAU as well as the project management led by Dr. P. Hartogh. Omnisys represents Sweden's contribution divided between the RU and the EU. The Laboratorium Satelitarnych Aplikacli Ukladow FPGA (CBK) represents Polish's contribution to the EU. RPG represents the second German's contribution focused on the amplification stage of the RU. The National Institute of Information and Communications Technology (NICT) represents Japan's contribution focused on the primary mirror manufacture of the TU and some components of the EU. The Institut of Applied Physics (IAP) University of Bern represents Switzerland's contribution focused on the optical test bench design to match the signal obtained by the TU into the RU.

All-solid-state Planar Schottky Diode technology has been chosen for the microelectronic MMIC chips that conform the LO multiplication chains and the frequency mixers for SWI. A passive cooling system is proposed to control temperature conditions of the SWI instrumentation between 120-150 K. It requires a bandwidth of a 20 % around the center frequency of each receiver with 100 MHz spectral resolution. The sensibility specifications proposed less than 1500 K of DSB noise temperature at 120-150 K for the 600 GHz channel and less than 4000 K for the 1200 GHz channel. LERMA got involved in SWI project in summer 2013 and it was in charge of the industrial delivery of two USO at 100 MHz and two K-band synthesizer of the SWI-EU to generate the initial LO chain bandwidth for each receiver between 22-26 GHz. LERMA was also in charge of the development and delivery of a frequency multiplier of the SWI-RU between 270-320 GHz to complete the LO multiplication chain of each receiver. Omnisys was in charge of the frequency mixers development and delivery for the 600 GHz channels. A contract between LERMA and Omnisys was closed within the framework of the SWI project. In summer 2014, LERMA got involved in the development of a 1.2 THz frequency mixer in the framework of the European SWI consortium. LERMA of the Observatoire de Paris in close collaboration with the *Laboratoire de Photonique et de Nanostructures* (LPN) of the *Centre National de la Recherche Scientifique* (CNRS) represent the French contribution to the SWI project. LERMA was in charge of the design, optimization and test of the developed modules while LPN-CNRS was in charge of manufacturing the modules. LERMA's contribution in the development of a 1.2 THz mixer prototype was initially supported by a contract between *Centre National d'Études Spatiales* CNES and LERMA-LPN, and this was complemented by this PhD work, fully supported by *Labex Exploration Spatiale des Invironnements Planétaires*

(Labex-ESEP) and granted to this author, Diego Moro Melgar. The CNES financial support and LERMAs commitment culminated with an ESA official contract that allowed LERMA to get involved in the 1.2 THz channel for SWI. LERMAs commitment in the CNES and ESA contracts was the demonstration of a PSBD-based 1.2 THz sub-harmonic frequency mixer able to fulfill the SWI specifications (less than 4000 K DSB noise temperature at 120 K). The challenge was proposed to both LERMA and Omnisys. The demonstration of the 1.2 THz channel feasibility was successfully accomplished by both groups at the beginning of 2016. The satisfactory results obtained by LERMA in the development of a 1.2 THz receiver culminated in summer 2016 with a full financial support by CNES of LERMA's contribution to the 1.2 THz channel delivery. However, the French contribution was not completely finished when this doctoral work was accomplish and further work on the final fly version of the 1.2 THz channel was required.

The author's work has been focused on the development of a PSBD-based 1.2 THz mixer design, a PSBD-based 600 GHz doubler design and the improvement of the PSBDs model for harmonic balance (HB) simulators. The chapter 2 of this work is dedicated to the physical model of PSBDs which is especially important at these high frequencies. It is due to the influence of additional phenomena associated to the reduced geometry and the saturation phenomena in the semiconductors. Regarding the author's role in LERMA's contribution, this author has been in charge of providing regular design reports of LERMA's progress to Omnisys in the framework of the LERMA-Omnisys contract. This author has presented LERMA's progress on the 1.2 THz receiver in the meetings taking place in Gothenburg (Sweden) between LERMA, Omnisys and ESA members. In addition, a consortium meeting was held every six months at MPS in Gottingen (Germany) between the different members of the consortium.

1.3 Design and Optimization of PSBD-based MMIC modules

The methodology followed in the design and optimization of PSBD-based MMIC modules for multiplication and mixing applications is briefly described in this section. Further details are referenced to previous works and documentation where it is detailed and discussed. The flowchart of the design and optimization process is illustrated in Fig. 1.3. It mainly consist on a three dimensional Computer-Aided Design (CAD) software with an Electromagnetic Field Simulator implemented to solve the Maxwell equations in a defined mesh of the 3D structure. These kinds of software are focused on the solution of the S-parameters of a structure that allow characterizing the losses associated to a specific geometry, materials and impedance matching. However, these kinds of software are not sufficient to carry out the optimizations of MMIC modules since the electrical behavior of active (oscillators) or passive (PSBDs, HBVs, SIS, HEB, etc) devices are not accounted for in HFSS simulations. The complementary software used in this work to develop the virtual design of each MMIC module is the so-called Advance Design System (ADS) software. It is an electronic design automation software system developed by Keysight Techonologies which is dedicated to RF, microwave and high speed digital applications. ADS software allows us to carrying out harmonic balance simulations of non-linear electronic circuits to obtain their frequency and time domain response. The CAD software that has been mainly used in this work is the High Frequency Simulation/Structure Software (Ansys-HFSS) [Ansys-HFSS 2016].

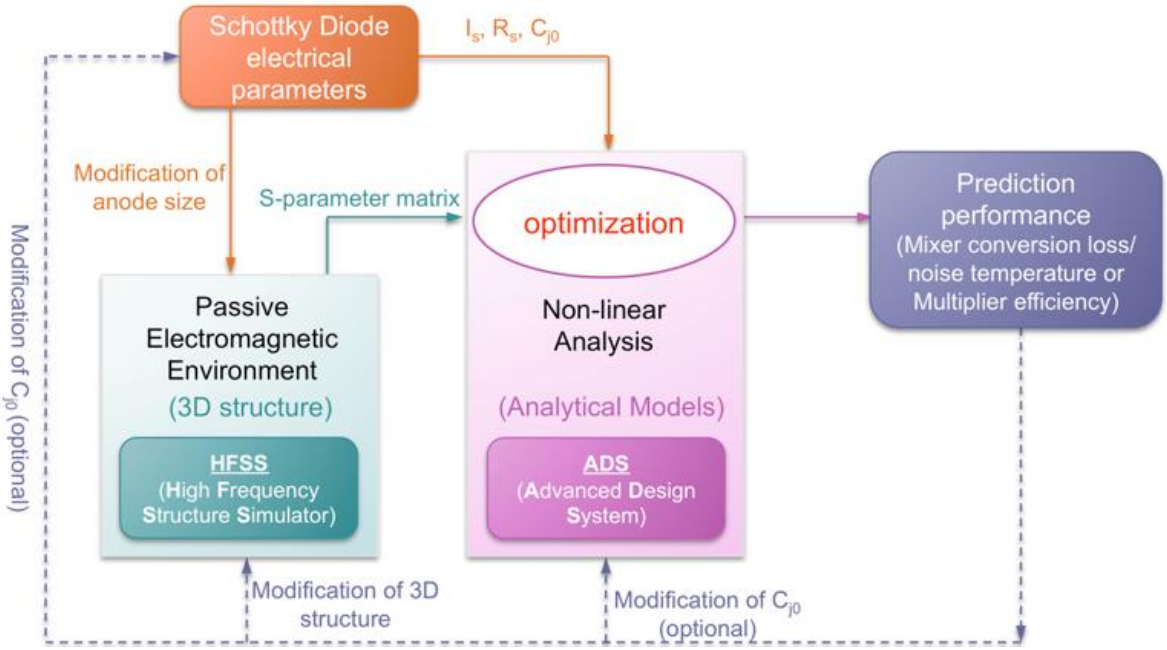

Fig. 1.3. Design flow chart based on Ansoft HFSS and ADS suite. Courtesy of Miss Hui Wang, March 2009.

HFSS has been especially important in this work to characterize the transmission/reflection coefficients (S-parameter) between waveguide transitions, the coupling efficiency of an antenna or probe with the input or output signal and the impedance matching network of the PSBDs devices. ADS software features the electrical model of a wide range of electronic devices (Schottky diodes, lumped elements, transistors, operational amplifiers, etc) and circuit elements (waveguides, transmission lines, attenuators, current/voltage/power sources, etc).

ADS software uses the S-parameters calculated by HFSS together with the electric models of the circuit elements and the analytical Schottky diode model to predict the performance of the structure. The analytical PSBD model main parameters are the saturation current I_S, the junction capacitance C_{j0} and the series resistance R_S. The analytical PSBD model used in this work will be thoroughly discussed in chapter two as well as the improvements included in terms of a two-dimensional Monte Carlo (2D-MC) simulator. The complementary utilization of both simulators allows the design and optimization of the MMIC modules developed in this work. The process is divided in two main stages. First, individual HFSS simulations of each impedance transition in the global structure are carried out to obtain the S-parameters of each transition of the circuit. Second, the ADS simulator is then used to simulate the transmission losses of a defined frequency signal in accordance with the calculated S-parameters, which contains each impedance transition, the materials properties of the simulated structure and the electrical path. These simulations allow the optimization of the structure in an iterative way to efficiently perform the required properties.

A. PSBD Frequency Multipliers

ADS-HFSS simulations of frequency multipliers for heterodyne applications are used to define the frequency and power range of the input and output LO frequency signals in the non-linear device. The design of frequency PSBD-based frequency multipliers using this methodology can be found in [Tuov95], [Maes05b], [Maes06b], [Sile09b], [Maes10a], [Maes10b], [Sile11a], [Sile11b], [Maes12], [Chen13], [Treu14]. The PSBDs' properties have to be carefully defined aiming for the maximization of the conversion efficiency of the input LO power into one of its harmonics. The input stage of the MMIC is fully optimized in ADS-HFSS simulations to maximize the coupling efficiency of the input LO power with the antenna or probe that matches the PSBDs of the chip. The output stage of the MMIC is fully optimized to enhance the *n*-th harmonic generation in the PSBDs and the coupling efficiency of the generated signal with the output antenna or probe that extracts the signal from the chip. Additional structures like filters, DC circuit and specific configurations of the PSBDs, are usually required in the design of frequency multipliers to correctly filter the undesired harmonics of the input LO signal. The bias of the PSBDs is usually required to efficiently manage the input power. HFSS simulations of the PSBDs in frequency multipliers are usually affected by non-linear electromagnetic fields and the near-field phenomena that arise when optimizing the input LO coupling efficiency. This makes the final optimization stage of frequency multipliers longer. These concepts are implemented on the design of a 600 GHz frequency doubler which has been developed by this author and detailed in Chapter 4.

B. PSBD Frequency Mixers

ADS-HFSS simulations of frequency mixers for heterodyne reception are used to define the correct interaction between the LO and RF input signals in the non-linear device to provide the IF signal. It is possible to find this methodology in the design of PSBD-based mixers [Thom10a], [Chen12], [Hanq12], [Treu16a], [Treu16b]. The PSBDs' properties have to be carefully defined in accordance with the available LO power and frequency range. ADS-HFSS optimization of frequency mixers is very complex since the objective of these

modules is coupling both the LO and the RF input signals in a specific frequency range. The PSBDs' sensitivity to detect the RF signal depends of a specific amount of LO power coupled with the diodes while the maximization of coupling efficiency of the RF signal and its conversion efficiency into the IF signal are especially important to reduce the noise temperature of the mixer. However, the LO and RF coupling efficiency are intimately related and the final conversion efficiency of RF signal into the IF signal by the PSBDs is a tradeoff between the LO and RF signals interaction. Additional structures like filters, DC circuits, IF adapter circuits and specific configurations of the PSBDs, are usually required in the design of frequency mixers to correctly filter the undesired frequencies and define the IF signal output path. The IF circuit adapter and DC circuit can be included in these mixer modules to improve the global performances. These concepts are implemented in the design of a 1200 GHz frequency doubler which has been developed by this author under the supervision of Dr. A. Maestrini and detailed in Chapter 6.

1.4 Structure and Objectives of this PhD Work

The THz science has achieved very important advancements during the last thirty years thanks to considerable technical developments that were used in recent space missions. The experiences, results and successes achieved have placed the multiplication technique as the most suitable way to reach this important frequency range with electronic-based devices. The high potential featured in Schottky technology in multiplications and mixing stages for space-borne applications has enhanced the development of these electronic devices. Schottky technology has usually been combined with superconductor technologies (SIS and HEB) for high sensitivity heterodyne reception, but all-solid-state PSBDs heterodyne receivers have proven to be the most suitable option when lower sensitivities are required. LERMA has had the opportunity to get involved in the development of the JUICE-SWI instrument and the success achieved within the framework of this project is now presented in this PhD. work.

The structure of this dissertation is divided into two different parts. The first part consists of a single chapter dedicated to the PSBDs devices. The improvement and systematization of the electrical PSBDs' modeling in this work has been carried out in terms of a Two-dimensional Monte Carlo (2D-MC) simulator. The improvements and their implementation in a simple analytical model are discussed in this part as well as the implementation of the analytical model in the Harmonic Balance ADS (HB-ADS) simulator. The second part consists of four chapters dedicated to each module developed by LERMA-LPN in the framework of SWI and the culmination of LERMAs work with a functional 1.2 THz receiver. The first chapter of second part is dedicated to the LERMA-LPN 300 GHz doublers, presenting the single and power-combined approach of this multiplier. The 300 GHz MMIC chips were designed before this work, but the experimental results provided by this module have been invaluable for validating the improved PSBD analytical model developed by this author. The second chapter of the second part is dedicated to the LERMA-LPN 600 GHz doubler. Two different versions are presented, discussed and compared. The design of the first version was developed by LERMA-LPN rather than by this author while the second version of this doubler has been fully designed by this author. Experimental results of this first version will discussed in this work. However, experimental results of the second version were not available yet. The design

of a second version of the 600 GHz doubler by this author was motivated by the additional LO power provided by the previous stage at 300 GHz during the development of the project. This second version is expected to provide additional LO power to pump the 1.2 THz mixer and ensure the availability of LO power in the full frequency band of the receiver. The third chapter of second part is dedicated to a LERMA-LPN 600 GHz mixer prototype that was designed before this work and has played a key role in the development of the 1.2 THz mixer. This module has provided the best performances reported at these frequencies using a PSBD-based mixer, and these results have been invaluable for the development of LERMAs contributions to SWI. The last chapter of second part culminates with the demonstration of the LERMA-LPN 1.2 THz receiver. The development of the 1.2 THz mixer is fully detailed and discussed in this section. The experimental results are analyzed, explained and validated by simulations. A novel study of the interaction between the LO multiplication chain and the mixing stage has been carried out by this author. This interaction has demonstrated to be critical in the prediction of the experimental performances of the receiver. Further improvements of the LO multiplication chain and the 1.2 THz mixer are finally proposed and discussed to enhance the LERMA's contribution to SWI.

Part 1: Planar Schottky Barrier Diodes Modeling

2 Analytical Model of Planar Schottky Barrier Diodes

This chapter is dedicated to the presentation of the physical model for the PSBDs used in this work. SBDs are well-known SC devices and the Bethe theory is a well-established analytical model to describe their electrical behavior. Important work has been developed during decades related with SBDs small-signal equivalent circuit models [Gonz97]. However, experimental devices are much more complex to describe, starting with two and three dimensional phenomena that can modify the ideal behavior described by Bethe's theory. Additionally, the PSBDs used in the THz modules developed in this work, function under large-signal conditions in which the validity of the small-signal equivalent circuit model is questionable. Theoretical research has been motivated by these phenomena, theoretical studies are available in the bibliography related with geometric phenomena [Dick67], [Cope70], [Geld91], [Louh94], [Moro16], fabrication process and defects [Call87], [Pére05], [Tung14] low temperature phenomena [Pad65], [Koll86], [Louh93], [Sieg91], [Hübe98], cyclostationary conditions [Shik04], [Pére04], [Graf10], saturation carrier phenomena [Graj00b], [Pard12], hot electron phenomena [Hjel90], etc. As a consequence, there is no consensus concerning the most suitable model of PSBDs for these experimental high frequency applications. This is mainly due to the high complexity of real phenomena, especially dynamic phenomena, that cannot be easily differentiated in experimental devices and they often interact with each to other. An additional complexity is associated with the commercial non-linear simulators, like ADS, that have not been specifically developed to take into account frequency dependent phenomena in the Schottky diode model. This results in a widespread use of a simple analytical model for SBDs simulations which is well described in this section since it is integrated into the ADS software.

The most common technique to simulate the SBD dynamic response in large-signal conditions is based on the so-called harmonic balance (HB) method [Gilm91a], [Gilm91b], [Rizz94]. The description of the electrical behavior of the device in terms of an analytical model is usually required by HB simulators, which provide the time and frequency domain response of the electrical device within a given circuit. Although HB simulations are able to provide the dynamic response of an electronic device under time-dependent excitations, static analytical models of the device are usually required by commercial HB simulators. This is the case of the HB simulations carried out with the ADS simulator within this work, where the electrical behavior of SBDs is given by the static current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the diode, which are incorporated by means of analytical equations that require to comply with continuity conditions at least up to their first derivate. These analytical functions are then applied to simulate the electric response in the circuit elements of the so-called Lumped Elements Circuit (LEC) model [Gonz97], [Pard14], that will be used to simulate the SBDs. The limitations imposed by commercial simulators has motivated important research work during last decades in the development of "in-house tools" for PSBDs modeling. The existence of frequency-dependent phenomena in Schottky diodes is well-known, especially at very high frequencies, where the transit time of the electrons can be in the same order of the signal period. Important advancements have been carried out by theoretical researchers specialized in Drift-Diffusion (DD) [Graj00a], [Graj04], [Sile05], Hydro Dynamic (HD) and Monte Carlo [Gonz97], [Pard12], [Pard15], [Pard16] models to simulate SBDs and shed light on non-equilibrium conditions. Further implementations of these theoretical models in HB simulators have notably contributed to improve the knowledge

about the operation of circuits based on SBDs under dynamic conditions. The MC simulator has demonstrated to be the most suitable method to study electronic SC devices since it is the only physical model that uses a microscopic approach to study the electrons' behavior. Very sophisticated MC simulators have been developed to account for all kind of dynamic phenomena associated to the electrons transport in SC devices. The most important challenge of MC simulators is the strong computational requirements to simulate these devices. However, extraordinary advancements have been carried out in this direction by Dr. J. Siles in [Sile05], [Sile09a] using an improved DD model for PSBDs and Dr. D. Pardo in [Pard15], [Pard16] with a MC simulator coupled with HB simulations. The main challenge of these advanced PSBDs models is their strong computational requirements and the difficulty to match them with the techniques used in experimental applications. The coupling of a one-dimensional MC simulator with HB simulations carried out by Dr. D. Pardo would not have been affordable for the practical development of this work due to the extremely demanding computational capacity required to perform such coupled MC-HB simulations of PSBDs in RF conditions. Additionally, one-dimensional simulations do not correctly describe the operation of real PSBDs in which 2D models can more accurately describe them, as discussed in this work. Based on the analysis carried out by Dr. J. Grajal in [Graj00a], [Graj00b] and Dr. J. Siles in [Sile08a], [Sile09a], we will try to optimize the properties of the PSBDs for the different modules developed by LERMA-LPN for specific multiplication and mixing applications.

The development of PSBD-based MMIC modules for submillimeter applications not only depends on the accuracy of the PSBDs electrical model but also on the accuracy of the simulation of the matching network system consisting of waveguides, transmission lines, antennas, probes, filters, etc. These requirements in the definition of the non-linear circuit simulations are carried out using commercial software, like ADS, which is not conceived to simulate only PBSD-based applications. This results in the widespread utilization of a simplified LEC model to simulate the electrical behavior of PSBDs within ADS. This simple model has been demonstrated to be useful to limit the computer requirements demanded by more sophisticate and accurate models while providing reasonable results. The LEC model has also been demonstrated to be accurate enough under certain conditions [Pard14], especially in varactor mode applications (typical of multipliers).

The objective of this chapter is to focus attention on the definition of a LEC model able to satisfactorily predict the performances of the developed PSBD-based modules and systematize the definition of the model parameters. The development of an analytical model for the I-V and C-V characteristics of the diode has been carried out in terms of a 2D-MC simulator that has been used to study the relationship between the different elements of the LEC model. The analytical equation of the capacitance model of PSBDs has been improved using our 2D-MC simulator to account for the two-dimensional phenomena that modifies the ideal capacitance given by Bethe theory. This 2D-MC simulator has also been useful to systematize the definition of the relationship between the C-V and I-V models of the PSBDs and to include them into a compact LEC to be implemented in non-linear circuit simulators like ADS.

2.1 The Two-Dimensional Monte Carlo Simulator

The *ensemble* MC simulators self-consistently coupled with a one/two-dimensional Poisson solver have demonstrated to be the most suitable tool in the study of modern ultra-scaled SC-based electronic devices [Mate15]. This is due to the microscopic approach to the Boltzmann's transport equation solution in SC materials together with a precise consideration of the topology of the devices. This simulator was provided by the Research Group on High-Frequency Nanoelectronic Devices of the University of Salamanca (http://nanoelec.usal.es/) and has been previously used for the simulation of several types of semiconductor devices. A one-dimensional version of this MC simulator was extensively used by this group for the study of III-V SBDs in [Gonz93], [Gonz97], [Shik04], [Pére04], [Pére05], [Shik06] and in Si-based SBDs in [Mart96], [Reng07], [Pasc07], [Pasc09]. It was extended to the current version of the 2D-MC simulator and extensively used in the study of HEMTs by Dr. J. Mateos [Mate99], [Mate00a], [Mate00b], [Mate04a], [Mate04b], [Vasa10] and was later modified by this author to include the gate leakage current in [Moro14]. This 2D-MC simulator has also proven its power in the study of ballistic devices [Mate03], [Iñig07] and self-switching nanodiodes [Iñig07], [Iñig08], [Iñig11] as well as in the experimental field as a powerful simulation tool for developing new applications at THz frequencies [Sang13], [Dahe16]. This 2D-MC simulator has been extensively used throughout this work to study PSBDs and develop the compact models that have been applied for the design of the multipliers and mixers fabricated in LERMA-LPN.

The flow chart of the *ensemble* 2D-MC simulations is illustrated in Fig. 2.1. The first point of a MC simulation is the definition of the SC physical properties, the SC layers and their geometries, the position of the metallic contacts and the physical parameters of the system (temperature, boundary conditions). Three non-parabolic spherical valleys (Γ, L, and X) are used to model the conduction band of the GaAs semiconductor layers [Fisc91]. The Schottky and the ohmic contacts as well as the boundary conditions of the structure are simulated as in [Gonz96], [Gonz97], [Mate00a], [Mate00b], [Mate04b], [Mate04b]. The Schottky contact is simulated as a perfect absorbing boundary, that is, all the carriers reaching the metal contact leave the structure and no carriers are injected from the metal into the semiconductor. This condition leads to the modification of the Maxwellian velocity distribution of the electrons at some tens of nanometers from the Schottky interface to a perfect hemi-Maxwellian distribution at the interface [Bacc76], [Mazi87], [Trav10]. Regarding the ohmic contact model, it imposes charge neutrality in the proximities of the electrode by injecting carriers with the appropriate thermal distribution (velocity-weighted hemi-Maxwellian) at the lattice temperature [Gonz97]. A mesh of the 2D structure is required to define the nodes where the Poisson equation is solved and the mesh where the electric field is calculated. The mesh size is defined in accordance with the Debye's length of the SC [Jaco89], which is around 1 to 5 nm in GaAs at the practical doping levels. A time discretization of the simulation using a time step, *dt*, is also required in ensemble 2D-MC simulations to define the instants at which the electrical field is updated and the data of each carrier is stored (both for having transient and average values of the different quantities: electron concentration, velocity, energy, electric potential and field, etc.). The choice of the time step is limited by the plasma frequency [Hock88] and the dielectric relaxation time [Tiwa92] of the SC, a value of around 1 to 2 fs is

usually used in our GaAs simulations. The initial number of particles and their position is defined in accordance with the doping of each mesh and the initial kinetic energy associated to each particle is randomly defined following the Maxwell-Bolzmann distribution. However the number of particles within the device changes during the simulation due to the entrance and exit of electrons through the electrodes. The total simulation time $T=N\cdot dt$ has to be also chosen, where N is the number of time steps to be computed before finishing the simulation. Once the structure is defined, the Poisson equation is solved by LU decomposition [Mate96] at T=0 to obtain the electric potential at each node of the mesh and the electric field in each cell. The particles' simulation loop is initiated by moving each electron during a random period of time under the electric field of the mesh where it is placed. The free flight time is randomly obtained in accordance with the energy dependent scattering probabilities of such electron in the defined SC (whose properties depend on the mesh where the electron is moving). When the free flight ends, if the time step has not finished, the electron suffers a scattering mechanism (considered instantaneous), that is also randomly selected according to the scattering probabilities associated with the energy of the electron at that time instant.

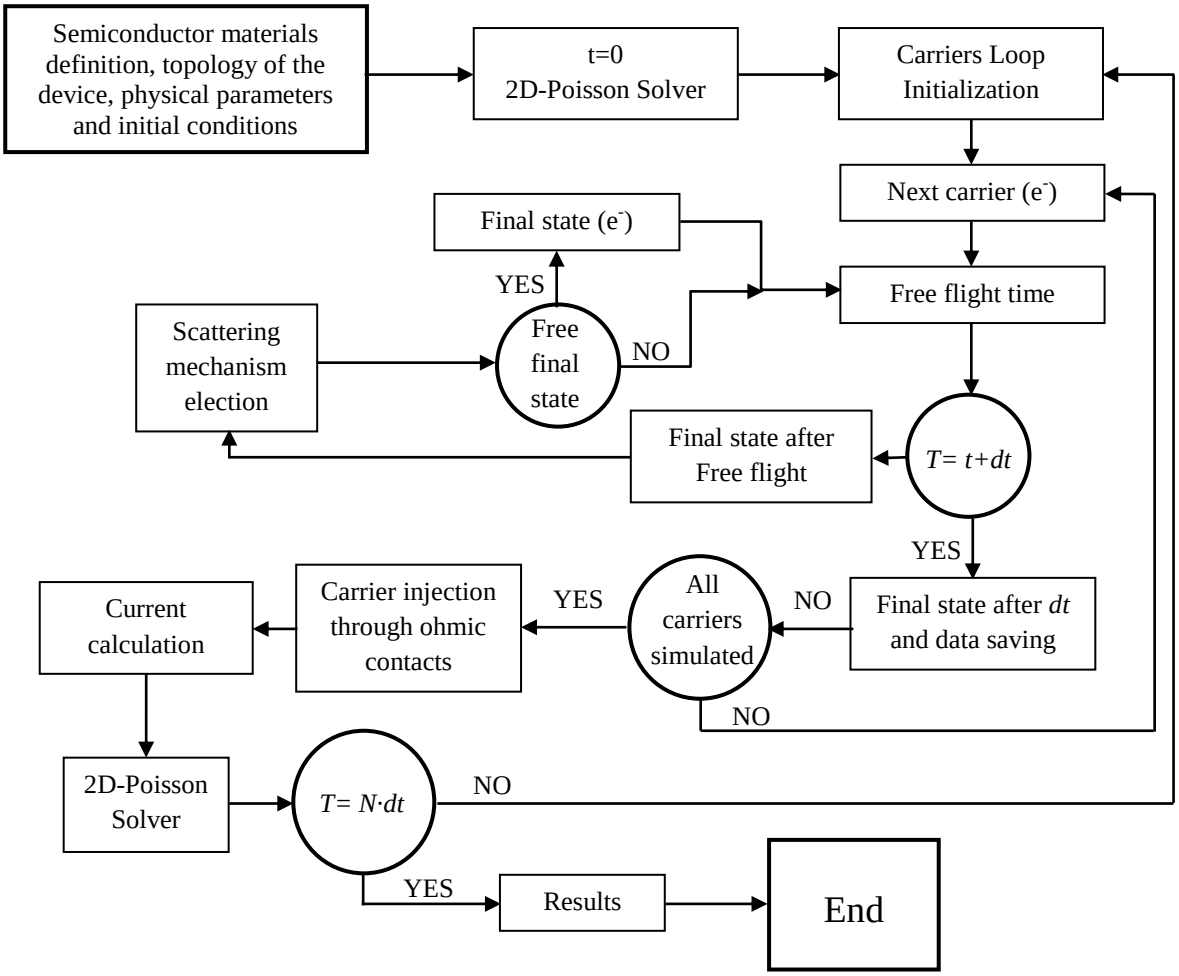

Fig. 2.1. The flow chart of our 2D-MC simulator.

We will consider ionized impurity, polar and non-polar optical phonon, acoustic phonon and inter-valley scattering mechanisms, whose probabilities are detailed in [Nag80], [Made81], [Ridl93] and the implementation of these processes in MC simulations in accordance with the carriers' energy is explained in [Boar80], [Jaco89]. Fermi–Dirac statistics, using a self-

consistent calculation of the Fermi level, are imposed for the occupancy of energy states by means of the rejection technique when selecting the final state after scattering events [Mate00a]. Once the scattering mechanism is selected, the next free flight is simulated and the process repeated until a complete time step *dt* is simulated for that particle. The loop continues until all particles have been simulated during that time step. After that the carriers are injected with a completely random rate (poissonian) through the ohmic contacts of the structure when the electron concentration is lower than the doping [Gonz96]. The current flowing through each contact is then calculated by computing the balance between the input and output particles during the simulated time step. The Poisson equation is then solved again in accordance with the current state of each particle within the simulation domain, and the particle loop starts again until the total number of time steps is simulated. More details about the MC simulator are presented in [Gonz97], [Mate00a], [Mate00b].

2.1.1 PSBD Structure in Monte Carlo Simulations

The simulated structure in this work is shown in Fig. 2.2 and described in [Moro16], which included in the Appendix of this dissertation. Taking advantage of the symmetry of the anode, only half of the diode is considered in the simulation domain for reducing the computational requirements. The GaAs layer structure consists of a highly doped n^+ substrate (with doping N_S) and an *n* epilayer (with lower doping N_E). The Schottky contact is placed on the top of the epilayer, while the ohmic contact is deposited on the semiconductor substrate and isolated from the epilayer by etching and dielectric deposition (Si_3N_4), which also passivates the global structure. The effect of the surface potential at the semiconductor interfaces of the device is modelled through a fixed negative surface charge density σ (which is a good approximation at low biasing) that provokes carrier depletion in its surroundings. The values of the surface charges σ placed at the epilayer–dielectric and substrate–dielectric interfaces (in red in Fig. 2.2) are calculated, for a given surface potential V_S as $\sigma=\sqrt{2qN_DV_S\varepsilon_{SC}}$ [Mate96], [Moro16], with N_D the doping level of each semiconductor layer, and ε_{SC} the permittivity of the SC. The simulated geometry resembles as closely as possible the fabricated PSBDs at LPN. The substrate thickness W_{Sub} and the ohmic contact length L_{OhmL} are large enough to ensure a flat potential profile at the bottom of the structure. The length of the dielectric region L_{Diel} that isolates the ohmic contact from the epilayer is similar to the epilayer thickness W_{EP}, and is determined by the technological process. The simulated Schottky anode size L_{SCH}, and the epilayer length L_{EP}, thickness, W_{EP}, and doping level, N_E, will be modified to study the influence of its geometry on the depletion region generated by the Schottky contact.

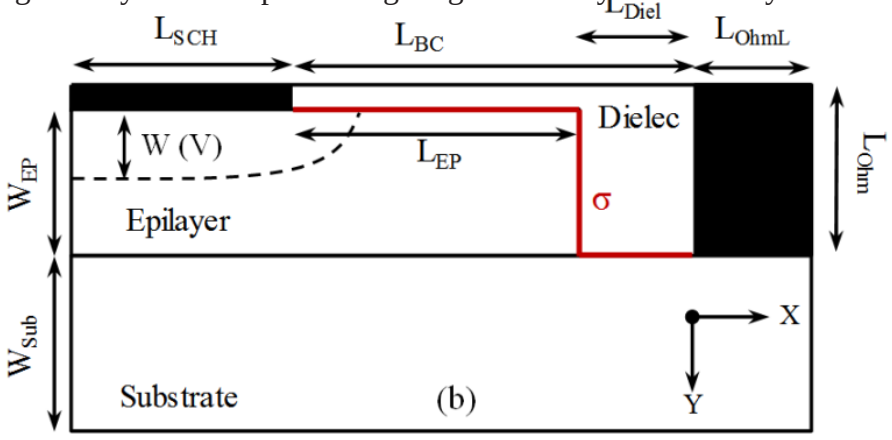

Fig. 2.2. Schematic of the MC simulation domain based on the real devices.

The structure defined in 2.2 is used in this work to carry out two different analysis of the PSBDs capacitance. First, the geometry of the epilayer (W_{EP}, L_{EP}) is defined according to its doping level to ensure that the depletion region does not reach the substrate layer or the vertical epilayer-dielectric interface placed at a distance L_{EP} from the edge of the anode. We will then study the impact of the surface charges on the depletion region of the Schottky contact [Moro16]. Next, a reduced epilayer thickness W_{EP} will be considered to study the impact of the substrate layer on the depletion region generated by the Schottky contact. The first study is significant for any PSBD since it accounts for 2D phenomena of the capacitance and includes the impact of surface charges in the epilayer-dielectric interface. The second study is dedicated to frequency mixing applications where the epilayer thickness of the PSBD has to be reduced as much as possible in order to optimize the value of the series resistance. As such, there is a risk that the depletion region enters into the substrate if the design is not correct or the input power is too high. As a consequence this effect should also be included into our C-V model.

Regarding the macroscopic magnitudes of current and capacitance used in this dissertation, it is important to mention that the definition of the Schottky contact in MC simulations doesn't account for either the barrier height of the contact or the built-in voltage appearing between two differently doped SC layers. This means that a correction value of the Schottky contact potential has to be added in post-processing to account for the barrier height and the built-in voltage between the SC layers. A correction value of 1 eV is always used within this dissertation since it leads to usual barriers height values in GaAs SBDs around 0.75 eV. This correction can be modified to match experimental PSBDs characteristics. A fix correction value for every 2D-MC simulation defines the barrier height independently of the doping of the epilayer SC. Although the dependency of the barrier height on the epilayer doping cannot be correctly analyzed on this way, a fix correction value allows studying the dependency of the barrier height with the geometry of the epilayer.

2.2 The Current Transport and Capacitance model in PSBDs

This section is dedicated to the theoretical model, based in Bethe theory, to describe the static electrical behavior of PSBDs. The band diagram of a Schottky contact [Sze06] is illustrated in Fig. 2.3. It is important to mention that the influence of barrier lowering [Sze06] due to image charge is not accounted for in this analysis. The Fermi level E_F of both the metal and the SC are at the same value in equilibrium conditions. $BC_{SC} \equiv E_C$ is the energy on the bottom of the conduction band, ϕ_m and ϕ_S are the work functions of the metal and SC (it is the energy between the vacuum level and the Fermi's level) and χ_m and χ_S are the electron affinities of the metal and SC.

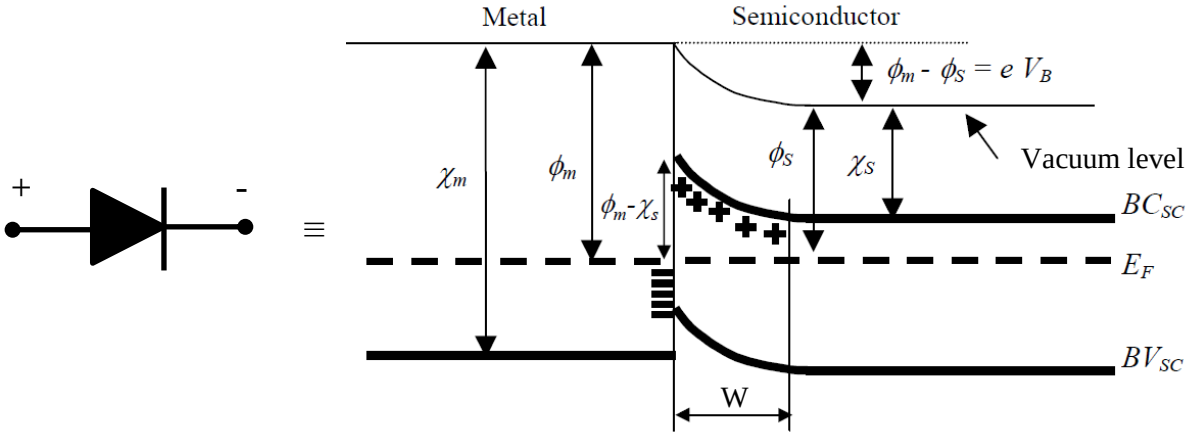

Fig. 2.3. Schematic of the conduction band in a Schottky Metal-SC contact at equilibrium, based on Bethe's theory [Sze06] and symbolical circuit representation of the SBDs.

The relationship between these magnitudes is given by,

$$\phi_S - \chi_S = -(E_F - E_C) = -q\phi_n \quad (2.1.a)$$

$$\phi_m - \phi_S = qV_B \quad , \quad (2.1.b)$$

$$\phi_m - \chi_S = \boldsymbol{q\phi_{Bn} = qV_B - (E_F - E_C)} \quad (2.1.c)$$

where $q\phi_n$ is the energy distance between the Fermi level and the bottom of the conduction band, $q\phi_{Bn}$ is the energy of the Schottky barrier and V_B is the built-in voltage of the Schottky contact. The built-in voltage of the junction naturally appears due to the different work functions of the metal and the SC. The built-in voltage induces a depletion of the SC electrons in the proximities of the junction with a depth *W*. The energy of the conduction band of the SC is modified in a value qV_d, where V_d is the voltage that drops in the depletion region generated under the anode, when biasing the Schottky contact of the diode. The depletion region increases as the bias V_d increases (reverse conditions) and very low current flows through the diode. On the other hand, when a positive bias is applied (direct conditions) the current increases exponentially as the depletion region is progressively reduced, until disappearing for flat band conditions $V_d = V_B = V_{FB}$. The variation of the depletion region size with the bias determine the value of the capacitance of the diode.

A. Bethe's Current Transport Analytical Model

The carrier transport through the Schottky contact is explained with the thermionic emission theory [Beth42], presented by Bethe in 1942. This theory demonstrated that the current density transport thought the Schottky barrier under reverse conditions features an exponential behavior. The current density through the barrier is the difference between the electrons that come out of the device from the SC to the metal and the electrons that enter

from the metal to the semiconductor [Gonz97]. The net current density through the Schottky contact is given by,

$$J_n(V_d) = A^* T^2 exp\left(-\frac{q\phi_{Bn}}{kT}\right) \cdot \left[exp\left(\frac{qV_d}{kT}\right) - 1\right] , \quad (2.2)$$

where A^* is the Richardson constant (~8 A·cm^{-2}K^{-2} in GaAs), T is the temperature, k is the Boltzmann constant and V_d is the bias that drops in the depletion region. It is experimentally observed that the current density when biasing above flat band conditions tends to a linear behavior due to the disappearance of the depletion region, and the current flowing through the diode is determined by the series resistance R_S of the device. Eq. 2.2 can be modified to reproduce this behavior as,

$$J_n(V_{bias}) = A^* T^2 exp\left(-\frac{q\phi_{Bn}}{kT}\right) \cdot \left[exp\left(\frac{q(V_{bias} - J_n(V_{bias}) \cdot R_S)}{kT}\right) - 1\right] , \quad (2.3)$$

where the voltage applied to the diode is calculated as $V_d = V_{bias} - J_n(V_{bias}) \cdot R_S$ in order to take into account the potential drop at the series resistance R_S. Eq. 2.3 tends to eq. 2.2 if $V_{bias} < V_{FB}$, since $J_n(V_{bias})$ is very low, while it tends to $J_n(V_{bias}) = V_{bias}/R_S$ if $V_{bias} > V_{FB}$.

B. Bethe's Capacitance Analytical Model

Regarding the capacitance model SBDs defined by Bethe's theory, this can be associated to the variation of charge induced by the depletion region when biasing the diode. The formation of the depletion region in a metal-n SC Schottky junction can be treated as a p$^+$-n SC-SC junction to solve the Poisson equation $\nabla^2\varphi = \rho$ [Sze06], where ρ is the charge density and φ is the electric potential. On one hand, the net charge within the depletion region, under the total depletion approximation, is $\rho \approx q \cdot N_E$. On the other hand, we assume that no modifications of the metal charge and the metal Fermi level are induced by the junction, i.e., ρ=0 and E=0 at the metal side. The analytical equation obtained for the depletion region depth is given by,

$$W(V_d) = \sqrt{\frac{2\varepsilon_{SC}(V_B - V_d)}{qN_E}} , \quad (2.4)$$

where ε_{SC} is the dielectric constant of the SC. The amount of depleted charge can be obtained from eq. 2.4 in accordance with the anode surface A,

$$Q(V_d) = -A \cdot qN_E \cdot W(V_d) = -A\sqrt{2q\varepsilon_{SC}N_E(V_B - V_d)} . \quad (2.5)$$

The capacitance of the junction is the charge variation per unit voltage, thus the analytical equation that describes the SBD capacitance in reverse conditions is given by,

$$C(V_d) = A\frac{dQ}{dV} = A\frac{\varepsilon_{SC}}{W(V_d)} = \frac{C_{j0}}{\sqrt{1 - \frac{V_d}{V_B}}} , \quad (2.6)$$

where C_{j0} is the so-called junction capacitance of the contact at V_d = 0 V, and it is given by,

$$C_{j0} = A\sqrt{\frac{q\varepsilon_{SC}N_E}{2V_B}} . \quad (2.7)$$

Eq. 2.6 describes the C-V characteristic of SBDs in reverse conditions and is valid for $V_d<V_B=V_{FB}$ but goes to infinite for $V_d=V_B$. This means that eq. 2.6 does not fulfill the continuity condition in the full voltage range. The implementation of the capacitance equation in harmonic balance simulations requires then additional considerations that will be discussed in next section.

C. Small Signal Equivalent Circuit in SBDs

Eq. 2.2 and 2.6 describes the capacitance and the current flowing through a Schottky contact in reverse conditions. The Small Signal Equivalent Circuit (SSEC) of the Schottky diode is illustrated in Fig. 2.4. An extended explanation of the SBD model can be found in [Tang13]. The SSEC of the Schottky junction is considered as a capacitance in parallel with a current source described respectively by eq. 2.2 and 2.6. The depletion region of the Schottky contact disappears as the bias goes from $V_{bias} < V_B$ to $V_{bias} = V_B$, and the current transport behavior of the diodes goes from exponential to linear behavior, as previously mentioned. This has usually been included in the SSEC of SBDs by considering an impedance in series configuration with the electrical model of the Schottky junction. Regarding the capacitance described by eq. 2.6, it is not important in DC bias conditions but it has a key role in RF conditions. Most of the current flowing through the SBD is determined by its capacitance if the time-dependent voltage signal does not exceed flat band conditions (varactor mode), and eq. 2.6 is able to describe this situation. The influence of the SBD capacitance in the current is strongly reduced if the flat band voltage is exceeded by the time-dependent voltage signal since most of the voltage drops in the series impedance (varistor mode). The analytical description of the DC current transport I_d in this SSEC of the diode is described by eq. 2.3.

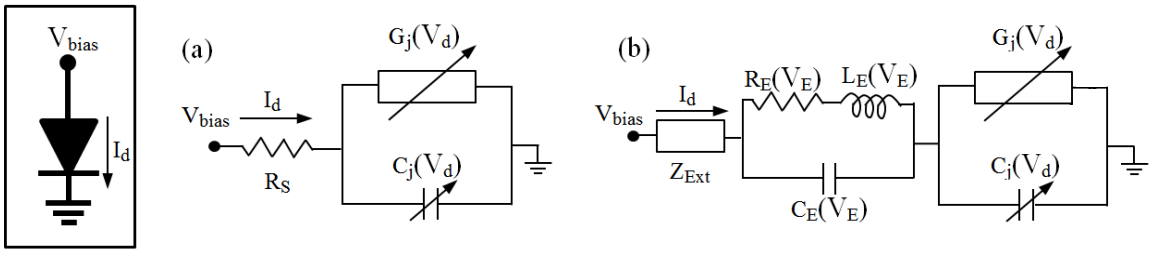

Fig. 2.4. Schematic of the small signal equivalent circuit of SBDs when considering (a) a pure real series resistance or (b) a complex series impedance.

Two different SSEC circuits have been illustrated in Fig. 2.4. The first SSEC shown in Fig. 2.4(a) is widely used by RF designers in the development of SBD-based circuits. It is usually found in the description of the diodes model in most of the multipliers and mixers modules mentioned in the references of this work and it considers a pure real series resistance. The second SSEC shown in Fig. 2.4(b) considers a complex impedance associated to the SC layers of the SBD. Some authors consider this an additional complex series impedance Z_{Ext} accounting not only for the ohmic contact resistance and parasites but also for frequency dependent resistive phenomena like the spreading resistance and skin effect [Dick67], [Cham78], [Louh95], [Chat11]. R_E, L_E and C_E are the resistance, inductance and capacitance that represent the SSEC of a SC [Gonz97], [Louh95]. Both circuits are equivalent in DC bias conditions and it is therefore possible to conclude that $R_S \equiv \text{Real}(Z_{Ext}) + R_E$ in certain voltage range, where R_E is associated to the epilayer resistivity and V_E is the voltage that drops in the epilayer SSEC. R_E is usually associated to the

epilayer thickness that is not depleted by the Schottky anode and it is therefore dependent on the voltage V_d that drops in the Schottky junction [Pard14]. The SSEC of the substrate SC of the SBD is not usually accounted for because its impedance is usually neglected compared to that of the epilayer. The first SSEC shown in Fig. 2.4(a) is the simplest model of the electrical representation of SBDs while the second model accounts for some frequency dependent phenomena. None of these SSECs are able to include the saturation phenomena or hot carrier transport.

The specific assumptions and PSBDs' model taken into account by this author will be discussed in the following sections.

2.2.1 Built-In Voltage and Barrier Height Relationship

The barrier height of the Schottky junction and the built-in voltage are closely related by the relations illustrated in (2.1). However, the values of these parameters are not usually given in the bibliography of experimental SBD applications, thus making impossible the comparison between different experimental diodes. The calculation of the position of the Fermi level, $q\phi_n=E_F-E_C$, in the SC is required now in order to understand the relationships given in eq.2.1. It can be obtained from the electron density in the SC [Swe06], as

$$n = N_c \cdot \frac{2}{\sqrt{\pi}} F_{1/2}\left(\frac{E_F - E_C}{kT}\right) \quad , \tag{2.8}$$

where N_C is the effective density of states in the conduction band and is given by,

$$N_c = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2} \quad . \tag{2.9}$$

E_F and E_C are the energies of the Fermi level and the bottom of the conduction band, m^* is the effective mass of the electrons ($m^*= 0.063m_0$ in GaAs), k is the Boltzmann constant, h is the Planck constant and T is the temperature of the semiconductor. $F_{1/2}$ is the Fermi-Dirac integral, which is typically redefined by considering $\eta=(E-E_C)/kT$, and is given by:

$$F_{1/2}\left(\frac{E_F - E_C}{kT}\right) = F_{\frac{1}{2}}(\eta_F) = \int_0^\infty \frac{\eta^{1/2}}{1+\exp(\eta-\eta_F)}\, d\eta \,. \tag{2.10}$$

The eq. 2.8 can by approximated by,

$$n = N_c \cdot exp\left(\frac{E_F - E_C}{kT}\right) \quad , \tag{2.11}$$

when the semiconductor is non-degenerated ($E_F-E_C < -3kT$), it means that $n < 0.05 \cdot N_C$, and accordingly,

$$q\phi_n(n,T) \approx E_F - E_C = kT \cdot ln\left(\frac{n}{N_C}\right) \quad . \tag{2.12}$$

It is important to note that eq. 2.12 is only valid when $n < 0.05 \cdot N_C$, with $N_C= 3.97 \cdot 10^{17} cm^{-3}$ at 300 K and $1 \cdot 10^{17} cm^{-3}$ at 120 K, in accordance with eq. 2.9. This means that a non-degenerated semiconductor at room temperature can become degenerated when cooling due to the reduction in the number of the available effective energy states in the conduction band. For this reason is important to obtain an equivalent expression of eq. 2.12 that considers the degeneracy of the SC. Due to the complexity of the Fermi-Dirac integral it is necessary to find some kind of analytical approximation. In [Aym81] we can find an analytical approximation of eq. 2.10 that allows defining a numerical non-linear equation for eq. 2.12 in degenerated

SCs. However, we can find a simpler analytical approximation in [Kro81] of eq. 2.12 for degenerated semiconductors given by,

$$q\phi_n(n,T) = (E_F - E_C) = kT\left(ln\left(\frac{n}{N_C}\right) + \sum_{i=1}^{\infty} a_i \cdot \left(\frac{n}{N_C}\right)^i\right) \quad , \tag{2.13}$$

where a very good approximation is obtained when considering the first four i-coefficients of the sum with a_1=3.5355·10^{-1}, a_2= -4.95·10^{-3}, a_3= 1.48·10^{-3} and a_4= -4.4·10^{-6}. Eq. 2.13 is not enough accurate if $n >> N_C$ and $T << 300$ K and The solution based in Aymerich [Aym81] can be required in that case. The relationship between the built-in voltage V_B and the Schottky barrier height $q\phi_{Bn}$ can be now defined using eq. 2.13 in eq. 2.1.

The values of $q\phi_n(N_E,T)$ are plotted in Fig. 2.5 when using the analytical expression of $F_{1/2}$ proposed in [Aym81] (solid lines) and the analytical approximation of E_F-E_C given by (2.13) (dashed lines). $q\phi_n(N_E,T)$ has been plotted with respect to the temperature at different epilayer doping. The analytical approximation given by eq. 2.13 is equivalent to Aymerich approximation at room temperature even at high doping but it differs as the temperature is reduced and the doping is increased. The selected epilayer doping range in Fig. 2.5 is based on the different doping used in this work for the development of PSBD-based modules for frequency mixing and multiplication. It is important to note that the non-degenerated SCs have a value of $q\phi_n$<-3kT, i.e, the Fermi level is lower than the conduction band energy while degenerated SCs feature a $q\phi_n$ > -3kT that becomes higher than the conduction band energy at n > $N_C(T)$. It is possible to conclude that a SC doped at 1·10^{17} cm^{-3} is non-degenerated at room temperature but it becomes degenerated when cooling down to ~250 K. A SC doped at 2·10^{17} cm^{-3} is degenerated even at room temperature and a SC doped more than 3·10^{17} cm^{-3} features a positive value of $q\phi_n$.

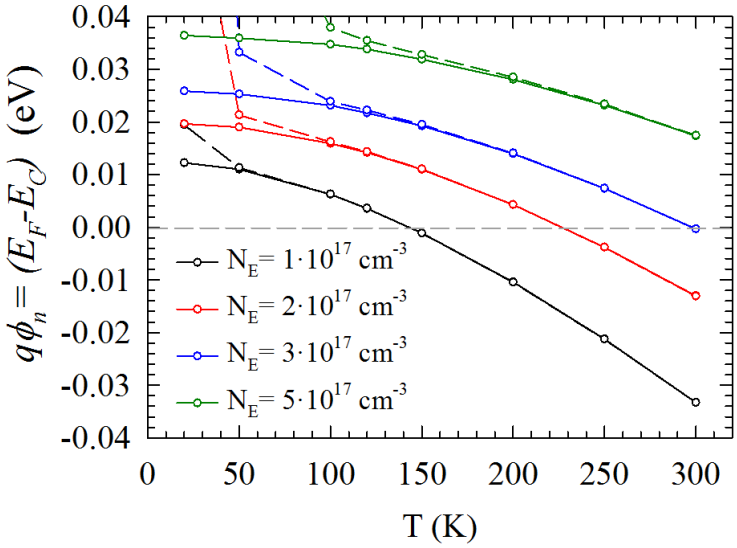

Fig. 2.5. Energy distance between the Fermi level and the conduction band E_F-E_C when varying the semiconductor doping level and the temperature. The numerical approximation is given by the solid lines and the analytical approximation by the dashed lines.

This relationship can by reinterpreted in terms of the built-in voltage and the Schottky barrier height. The barrier height is therefore bigger than the built-in voltage when the semiconductor is non-degenerate. However, the difference between the barrier height and the built-in voltage is reduced as the doping increases, and it is finally inversed from n > $N_C(T)$, when the barrier height becomes lower than the built-in voltage for high degenerated semiconductors,

$$qV_B < q\phi_{Bn} \quad \text{for} \quad E_F < E_C$$
$$qV_B > q\phi_{Bn} \quad \text{for} \quad E_F > E_C \quad . \tag{2.14}$$

The qualitative relationship between the built-in voltage and the barrier height is defined by eq. 2.14 and an approximation of the value is obtained using eq. 2.13 in eq. 2.1. It has been mentioned that the barrier height of experimental PSBDs depends on the fabrication process as well as the metal annealing used to generate the Schottky contact [Tung14]. However, the relationship between the built-in voltage and the barrier height remains. It is possible to use this relationship to theoretically compare PSBDs with different doping levels or at different temperatures if a good reliability of the fabrication process of the PSBDs is achieved. This defines the main relationship between the C-V and I-V curve of any Schottky diode and it allows obtaining both physical parameters from the experimental measurement of one of them [Pado65], [Koll86], [Hje90]. This relationship will be used throughout this work when defining the properties of the PSBDs from the experimental measurement of the I-V characteristic.

2.2.2 Analytical Model of Current Transport in PSBDs

The analytical model used to simulate the DC current transport through the Schottky junction of PSBDs is discussed in this section. SBDs experimentally show additional real phenomena that induce a reduction in the slope of the exponential I-V curve given by eq. 2.2. This effect was studied by Padovani in [Pado65], where the comparison of experimental results of SBDs with eq. 2.2 when varying the temperature of the device is carried out. The approach proposed by Padovani has lately become widespread in the experimental community. Padovani proposes the introduction of a corrected temperature $T'=T+T_0$ in the exponential terms of eq. 2.2, where T is the temperature of the device and T_0 is a parameter that allows to fit the experimental measurements of the SBD DC current. This approach was lately redefined in terms of an additional parameter in eq. 2.2, the so-called ideality factor $\eta \geq 1$, where $T'=\eta T=T+T_0$. This experimental approach was discussed by Kollberg in [Koll86] where the ideality factor is defined as $\eta=\theta/T$. The ideality factor is used by Kollberg to study several experimental devices and it is compared at different temperatures. Kollberg demonstrates that the ideality factor increases as the temperature of the device decreases. The analytical equation used by this author is based in Padovani's approach but considering Kollberg's definition of the ideality factor. This results in:

$$J_n(V_d) = A^* T^2 exp\left(-\frac{q\phi_{Bn}}{k\theta}\right) \cdot \left[exp\left(\frac{qV_d}{k\theta}\right) - 1\right] = J_S\left(exp\left(\frac{qV_d}{k\theta}\right) - 1\right) , \tag{2.15}$$

where the saturation current density is defined as,

$$J_S(V_d) = A^* T^2 exp\left(-\frac{q\phi_{Bn}}{k\theta}\right) \quad \text{with} \quad \theta = \eta T \quad . \tag{2.16}$$

The only difference between eq. 2.16 based in Padovani's equation and Kollberg's equation is the definition of the saturation current density. Kollberg proposes to also replace the J_S square dependence on the temperature by θ^2. Different definitions of the analytical equation can be found in the bibliography, for example in [Hübe98] and [Hard99]. The only difference with the proposed equation eq. 2.15 is the predicted barrier height from the experimental measurements. These approaches were compared by this author using the described 2D-MC simulations (not included in this work) at different simulated temperatures of PSBDs (Fig. 2.2) and Padovani's approach shows a better agreement between the different simulations.

However, the only difference between these analytical equations is the predicted barrier height $q\phi_{Bn}$ from the experimental fit of the SBD current. This is demonstrated in [Hübe98] and [Hard99] that the built-in voltage dependence in the temperature features a linear behavior and the ideality factor increases as the temperature decreases. It is important to note, for the reader, that the relationship between the built-in voltage and the barrier height used by Hübers and Hardikar are associated to non-degenerated SC while some of the presented experimental diodes are degenerated.

Coming back to eq. 2.15 and eq. 2.16, no image charges are considered in our model in order to simplify the theoretical analysis of experimental PSBDs. This assumption leads to a slight underestimation of the barrier height of around 10 to 20 mV, as analyzed in [Hard99]. This deviation affects the predicted value of the built-in voltage from the experimental measurements of the I-V characteristic. It is necessary to correct in that quantity the calculated built-in voltage when using eq. 2.13 in eq. 2.1, but a deviation of 10 to 20 mV in the defined built-in voltage does not have a notable impact on the performances of a full PSBD-based module. Tunnel effect is not considered in the analysis carried out in this work, since the conditions in which it is significant are actively avoided in the design of PSBD-based modules. The tunnel effect is associated to the appearance of the so-called breakdown voltage V_{BR} at high reverse bias conditions, which is always avoided in multiplication and mixing PSBD-based modules [Schl01b]. It is due to the degradation of the PSBDs associated to a time-dependent voltage signal that exceeds the breakdown voltage of the device while operating in RF conditions. Eq. 2.15 will be used within this work to fit the experimental I-V measurements of fabricated PSBDs and it will allow us to estimate the barrier height of the Schottky contact and thus, the built-in voltage using eq. 2.13 in eq. 2.1.

2.2.3 Resistance Model of PSBDs

Eq. 2.15 together with the series resistance model define the DC electrical behavior of PSBDs. The constant series resistance R_S proposed in Fig. 2.4(a) has been used within this work to fit the DC measurements of the I-V characteristics in the fabricated PSBDs. This simple model is widely used by RF engineers and it allows matching the experimental I-V characteristics of PSBDs from some hundreds of mV to flat band conditions. 2D-MC simulations of the I-V characteristics of several PSBD structures have been performed and fitted with eq. 2.15 and a constant series resistance to illustrate this process. The physical and geometrical parameters of these simulated structures are given in Table II.1

Symbol	Diode1	Diode2	Diode3	Diode4	Diode5
L_{SCH} (nm)	1000	600	680	200	200
W_{EP} (nm)	350	350	250	55	55
L_{EP} (nm)	460	460	300	230	230
L_{Diel} (nm)	240	240	150	120	120
L_{BC} (nm)	700	700	450	350	350
W_{Subs} (nm)	500	500	500	350	350
N_E (cm^{-3})	$1\cdot10^{17}$	$1\cdot10^{17}$	$2\cdot10^{17}$	$3\cdot10^{17}$	$5\cdot10^{17}$
N_S (cm^{-3})	$5\cdot10^{18}$	$5\cdot10^{18}$	$5\cdot10^{18}$	$5\cdot10^{18}$	$5\cdot10^{18}$
V_S(V)	-0.5	-0.5	-0.5	-0.5	-0.5

Table II.1. Physical and geometrical parameters of five simulated PSBD structures in 2D-MC simulations.

Diode1 is based on the diodes used in a 300 GHz doubler module presented in Chapter 3, while Diode2 and Diode3 are based in the diodes used in the 600 GHz doublers presented in Section 4.1 and Section 4.2, respectively. Diode4 and Diode5 are based in the diodes used in the 1.2 THz mixer developed in Chapter 6.

The simulations of Diode1 at 150 nm, 250 nm and 350 nm epilayer thickness are plotted and compared in Fig. 2.6. The largest epilayer thickness has been chosen to match the depth of the depletion region when biasing at the breakdown voltage experimentally observed in LPN PSBDs. The 2D-MC simulations allow obtaining the I-V characteristics of the structure in A/m at bias higher than ~0.45 V. Lower currents are difficult to be attained by this 2D-MC model due to the small number of particles leaving the structure and the lack of statistical data to have a precise value (simulation time should be unpractically increased). MC results have been multiplied in this section by a non-simulated length L_1 that allows transforming the MC current per unit length into absolute current data accounting for a certain anode surface, and to have the values of the saturation current and series resistance in A and Ω, respectively. The results presented in Fig. 2.6 use the 2D-MC data obtained for Diode1 structure to have an approximation of the saturation current and series resistance of a 17 μm^2 anode surface. This is the anode surface of the PSBDs used in our 300 GHz doubler presented in Chapter 3. The red line is given by eq. 2.15, used in the junction current model of the SSEC in Fig. 2.4(a), and the blue line is the result of including the series resistance R_S in the SSEC. In the last case the values of the saturation current I_s, the barrier height $q\phi_{Bn}$, the ideality factor η and the series resistance are indicated.

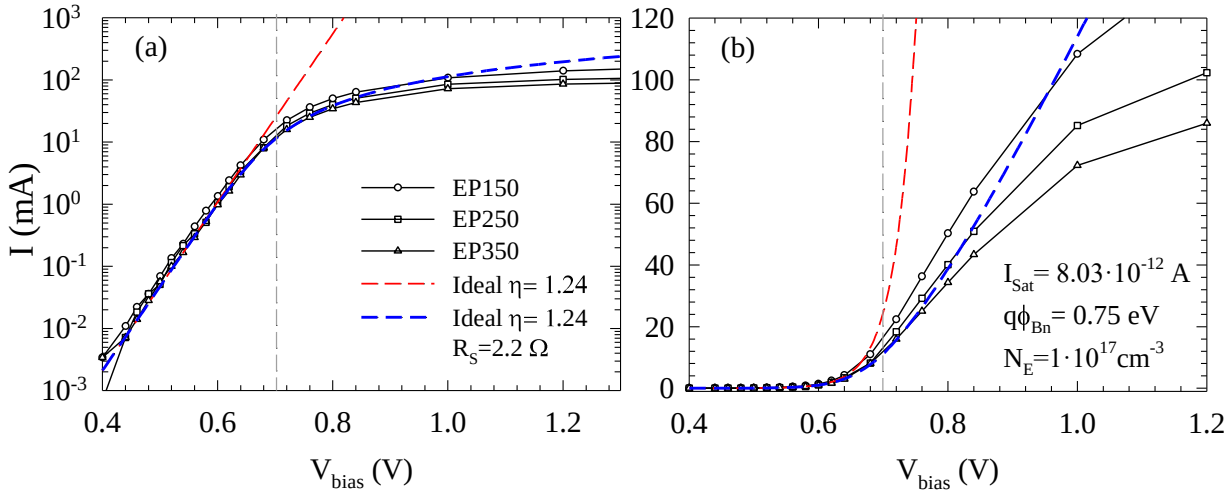

Fig. 2.6. 2D-MC I-V characteristics of Diode1 structure in (a) logarithmic and (b) linear scale when considering 17 μm^2 anode surface at 150 nm, 250 nm and 350 nm epilayer thickness. The legend affects both graphs. Blue line fits the EP350 case with I_{Sat}= 8.03·10^{-12} A, $q\phi_{Bn}$= 0.75 eV, η=1.24 and R_S= 2.2 Ω. The value of the flat band voltage is indicated by the dashed grey line at 0.7 V.

It is possible to view in Fig. 2.6(a) the exponential behavior of the current at bias lower than flat band and how it tends toward a linear behavior, Fig. 2.6(b), above flat band (0.7 V). The slope reduction of the I-V characteristic for $V_{bias}>>V_B$ is associated to hot electrons that get energy enough to reach higher valleys of the conduction band with smaller effective mass and conductivity. No tunnel effect or image charges are accounted for in our 2D-MC simulator but the obtained I-V characteristics feature an ideality factor larger than one. Some slight variations in the barrier height are found between different simulations, as indicated in Table

II.2, but the relationships described in eq. 2.1 have been verified in all cases. It is possible to note in Fig. 2.6(b) that the SSEC illustrated in Fig. 2.4(a) is able to fit the I-V characteristics up to flat band but not above. The 2D-MC simulations are able to give us an approximation of the SC layers resistivity but do not take into account additional resistance sources like the ohmic and Schottky metallic contacts, fabrication defects or frequency dependent resistances like the previously mentioned skin effect resistance. This means that any value of series resistance given by this 2D-MC simulator is always smaller than the experimental series resistance of PSBDs.

The same analysis is carried out in Fig. 2.7 and Fig. 2.8 for Diode2 and Diode3, respectively. Diode2 is equivalent to Diode1 but the simulated anode length L_{SCH} is smaller. Diode3 is equivalent to Diode2 but with a double epilayer doping and a similar anode size. The 2D-MC results plotted in Fig. 2.7 consider a 3.5 μm^2 anode size and Fig. 2.8 consider a 3.25 μm^2 anode size. This is the anode surface of the PSBDs used in our 600 GHz doublers that will be presented in Sections 4.1 and 4.2, respectively.

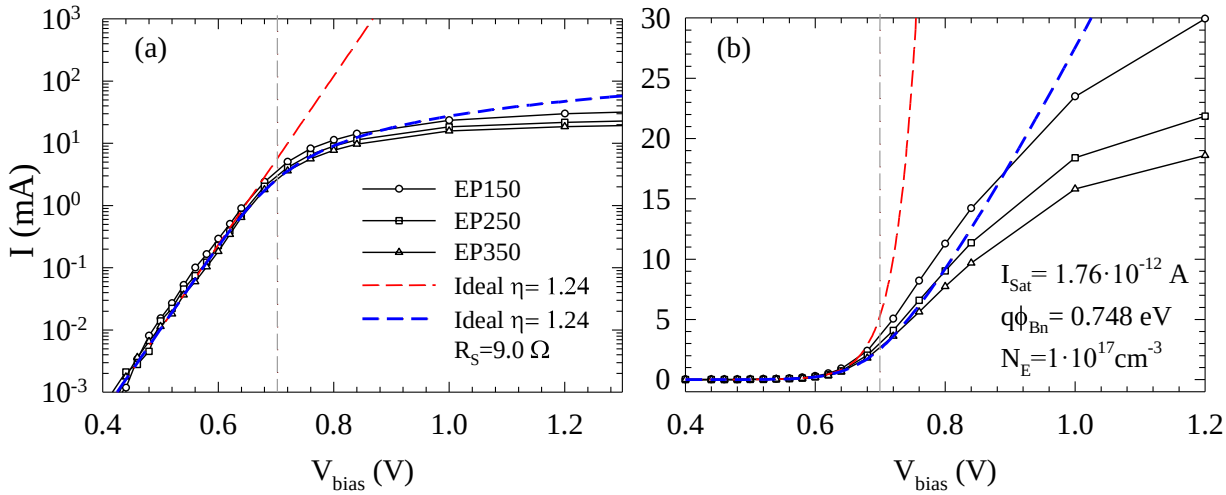

Fig. 2.7. 2D-MC I-V characteristics of Diode2 structure in (a) logarithmic and (b) linear scale when considering 3.5 μm^2 anode surface at 150 nm, 250 nm and 350 nm epilayer thickness. The legend affects both graphs. Blue line fits the EP350 case with I_{Sat}= 1.76·10^{-12} A, $q\phi_{Bn}$= 0.748 eV, η=1.24 and R_S= 9 Ω. The value of the flat band voltage is indicated by the dashed grey line at 0.7 V.

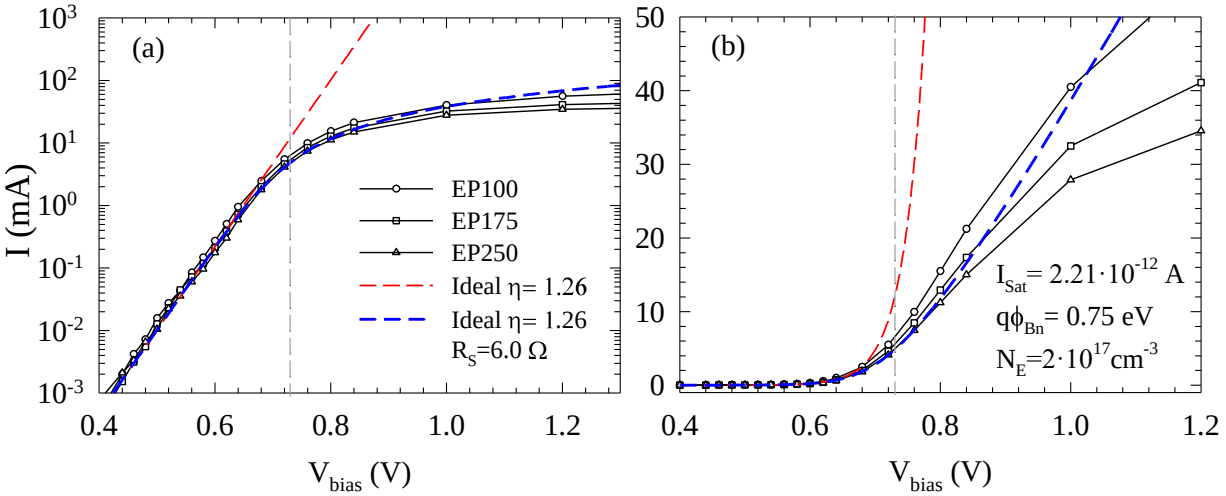

Fig. 2.8. 2D-MC I-V characteristics of Diode3 structure in (a) logarithmic and (b) linear scale when considering 3.25 μm^2 anode surface at 100 nm, 175 nm and 250 nm epilayer thickness. The legend affects

both graphs. Blue line fits the EP350 case with I_{Sat}= 2.21·10^{-12} A, $q\phi_{Bn}$= 0.75 eV, η=1.26 and R_S= 6 Ω. The value of the flat band voltage is indicated by the dashed grey line at 0.73 V.

The results of Diode2, Fig. 2.7, are equivalent to the results for Diode1 presented in Fig. 2.6, but the reduced anode size leads to a higher series resistance and a smaller saturation current. The current model parameters used to fit each I-V characteristic are indicated in Table II.2. The results of Dode3, Fig. 2.8, are equivalent to those of Diode2, Fig. 2.7, but the increment in the epilayer doping induces a reduction of the series resistance and an increment of the saturation current.

Regarding the PSBDs that will be used for the 1.2 THz mixer, the 2D-MC I-V characteristics obtained at 55 nm, 75 nm, 95 nm and 145 nm epilayer thicknesses are plotted in Fig. 2.9 and 2.10 for Diode4 and Diode5 structures respectively. These two structures are equivalent but the epilayer doping is 3·10^{17} cm^{-3} for Diode4 and 5·10^{17} cm^{-3} for Diode5. The 2D-MC results presented in Fig. 2.9 and 2.10 correspond to a 0.2 μm^2 anode size.

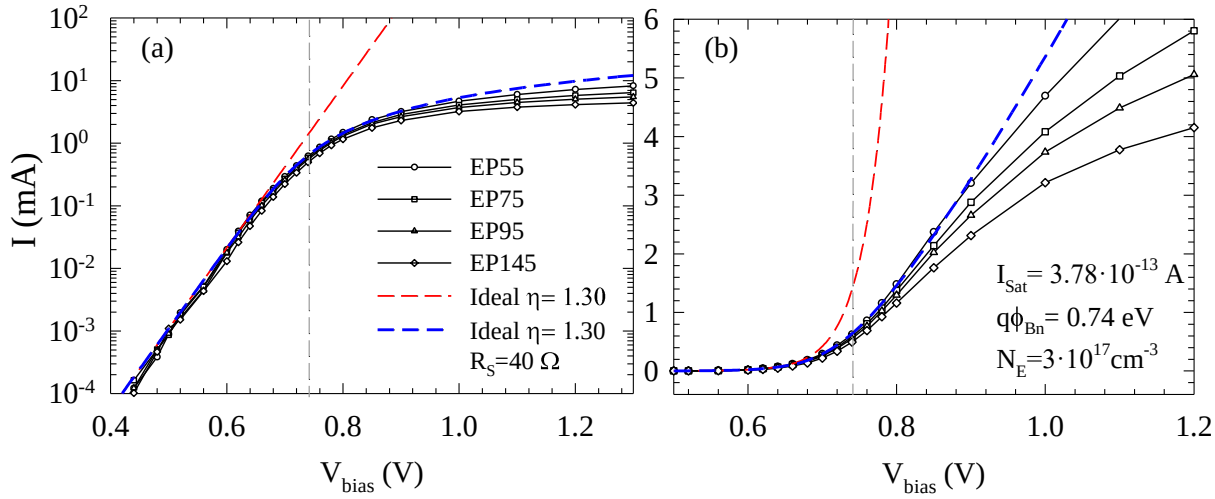

Fig. 2.9. 2D-MC I-V characteristics of Diode4 structure in (a) logarithmic and (b) linear scale when considering 0.2 μm^2 anode surface at 55 nm, 75 nm, 95 nm and 145 nm epilayer thickness. The legend affects both graphs. Blue line fits the EP55 case with I_{Sat}= 3.78·10^{-13} A, $q\phi_{Bn}$= 0.74 eV, η=1.3 and R_S= 40 Ω. The value of the flat band voltage is indicated by the dashed grey line at 0.74 V.

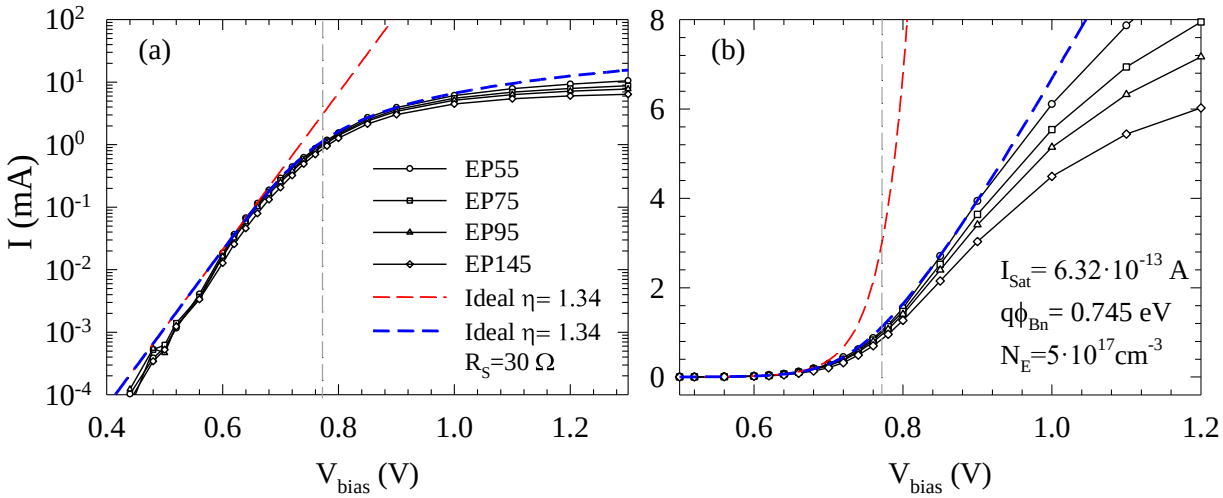

Fig. 2.10. 2D-MC I-V characteristics of Diode5 structure in (a) logarithmic and (b) linear scale when considering 0.2 μm^2 anode surface at 55 nm, 75 nm, 95 nm and 145 nm epilayer thickness. The legend affects both graphs. Blue line fits the EP55 case with I_{Sat}= 6.32·10^{-13} A, $q\phi_{Bn}$= 0.745 eV, η=1.34 and R_S= 30 Ω. The value of the flat band voltage is indicated by the dashed grey line around 0.765 V.

The ideality factor is accurately estimated by the simulations presented in Fig. 2.9 and it is slightly higher than in Diode2 and Diode3. The series resistance has also notably increased for Diode4 and the saturation current has decreased due to the small anode size. The results obtained for Diode5, Fig. 2.10, are equivalent to those of Diode4, Fig. 2.9, but the series resistance has decreased and the saturation current has increased due to the higher epilayer doping. It is interesting to note that the constant series resistance model used to fit the I-V characteristic presented in Fig. 2.6 to 2.10 works better after flat band for Diode4 and Diode5. The set of parameters used in the current model to match every 2D-MC simulated I-V characteristic are gathered in Table II.2. It is possible to note a dependency of the ideality factor with the doping level of the epilayer. The increment of the doping leads to an increment of the ideality factor. This means that the ideality factor is related to the relationship between the Fermi level and the conduction band energy described by eq. 2.8. However, further analysis would be required to precisely study this dependency. The saturation current density given by eq. 2.16 has been included in Table II.2.

Symbol	W_{EP} (nm)	N_E ($10^{17}cm^{-3}$)	η	I_{Sat} (pA)	J_{Sat} (A/m^2)	R_s (Ω)	$q\phi_{Bn}$ (eV)	V_B (V)
Diode1	150	1	1.24	11.32	0.663	1.65	0.739	0.693
	250	1	1.24	9.10	0.533	1.95	0.746	0.700
	350	1	1.24	8.03	0.471	2.20	0.750	0.704
Diode2	150	1	1.24	2.47	0.706	6.7	0.737	0.691
	250	1	1.24	1.99	0.567	8.0	0.744	0.698
	350	1	1.24	1.76	0.501	9.0	0.748	0.702
Diode3	100	2	1.26	3.01	0.927	4.6	0.740	0.723
	175	2	1.26	2.35	0.725	5.1	0.748	0.731
	250	2	1.26	2.21	0.682	6.0	0.750	0.733
Diode4	55	3	1.30	0.38	1.865	40.0	0.740	0.736
	75	3	1.30	0.35	1.706	42.2	0.743	0.739
	95	3	1.30	0.33	1.607	44.0	0.745	0.741
	145	3	1.30	0.28	1.385	47.0	0.750	0.746
Diode5	55	5	1.34	0.63	3.115	30.0	0.745	0.763
	75	5	1.34	0.60	2.941	33.0	0.747	0.765
	95	5	1.34	0.56	2.776	34.5	0.749	0.767
	145	5	1.34	0.46	2.268	36.5	0.756	0.774

Table II.2. Current model parameters used to match the different PSBD structures simulated with the 2D-MC simulator and presented in Fig. 2.6 to Fig. 2.10.

It is possible to note in Table II.2 that the saturation current density depends on the simulated L_{SCH} anode length. The smaller the anode width L_{SCH} is, the higher the saturation current density of the Schottky contact. This is because the current distribution along the L_{SCH} length of the anode is not homogenous but it is higher in the edge of the anode. This leads to higher saturation current densities in long rectangular anodes than in square anodes. This qualitative behavior can be also extended to circular anodes. The modification of the saturation current density when changing the epilayer thickness affects the calculation of the barrier height and therefore the built-in voltage of the contact. This is because the eq. 2.16 is defined for one-dimensional structures where the current flux distribution is homogenous in

every point of the contact. However, these observations related to the saturation current density change when varying the epilayer thickness are not sufficiently large to dramatically affect the prediction capabilities of the model for RF applications. When comparing the values of the predicted series resistance of the PSBDs obtained with 2D-MC simulations with the experimental values of the fabricated diodes, we have observed that the simulated value is usually between 40-60 % of the one extracted with the experimental measurements. As a result, half of the experimental series resistance R_S is attributed to the epilayer resistance R_E as approximation in the analysis performed within this work, while the rest will be associated to parasitic contacts resistances.

We have to note that the value of R_S required to match 2D-MC simulations of the I-V, is smaller than the resistance of the linear part of the curve in all simulations carried out. The SSEC model presented in Fig. 2.4(a) fits the I-V characteristics up to flat band conditions and it is the best reference when measuring PSBDs characteristics. We can interpret the R_S lumped element of the SSEC as a simple mathematical parameter used in the electrical model to fit the I-V characteristic. This fact has been previously noted in [Penf62], [Burc65], [Lips98] where the value of R_S is proposed to be voltage dependent and associated to the non-depleted epitaxial region. The consideration of a constant series resistance is a good approximation when studying frequency multipliers because they are designed to be excited by voltage-dependent signals that do not exceed the flat band voltage. However, the implementation of a variable series resistance can be especially important when studying frequency mixers in order to fit the I-V characteristic beyond flat band. Based in [Lips98] the variable series resistance associated to the non-depleted epitaxial region can be generalized as:

$$R_S(V_d) = \begin{cases} r_{S;Max} \cdot [W_{EP} - W(V_d)] \; ; & V_d < V_B \\ r_{S;Max} \; ; & V_d > V_B \end{cases} \quad with \; r_{S;Max} = \rho / A \quad , \qquad (2.17)$$

where W_{EP} the epilayer thickness, $W(V_d)$ is given by eq. 2.4, ρ is the resistivity of the SC and A the anode size. The series resistance given by eq. 2.17 is only associated to the epilayer and the value $r_{S;Max}$ can be used as adjustable parameter to fit experimental PSBDs characteristics. In this case, the value $r_{S;Max}$ will be always higher than the series resistance used with the constant series resistance model. This variable series resistance model allows acceptable fitting of the I-V characteristics at higher voltages than those reached by the constant series resistance model. If this improved model is used for the simulation of the mixer modules the predicted performances are decreased with respect to those obtained with the constant series resistance. This is because the matching of the I-V obtained with the variable series resistance reproduces better the linear part of the I-V, which is higher than the value used in the constant series resistance model. However, the use of this variable series resistance model in this dissertation was finally discarded because its implementation in the analysis of mixers was difficult to support with experimental results since the linear part of the I-V is difficult to be measured due to the high current values provided by the PSBDs and the associated self-heating distorts the measurements in a way that is difficult make conclusions. Additionally, no hot electron phenomena are accounted for in this PSBD analytical current model, thus making it impossible to compare it with the experimental results in this region of the curve. Nevertheless, this analysis enhanced the development of the SSEC presented in Fig. 2.4(b) by different authors. The series resistance given by eq. 2.17 is related to the epilayer resistivity

and associated to the lumped element R_E in that model. The RLC series impedance model indicated in Fig. 2.4(b) will be discussed later in this section. Any additional source of impedance is included in Z_{Ext}.

2.2.3.1 Extrapolation of the Series Resistance

One of the most difficult questions to be answered when modeling and optimizing the physical properties of the diodes required in a specific application is the value of the series resistance that has to be considered for different PSBDs. This question is discussed here and the method used by this author is presented. It is important to note that this method cannot be applied to PSBDs fabricated with different technological processes. The assumption proposed by this author is based in the reproducibility of the PSBDs fabrication process at LPN. A widely-used method to estimate the series resistance of a hypothetical PSBD is based on the well-known inverse proportionality relationship between the resistance and capacitance of a Schottky anode. The larger the anode size is, the larger the junction capacitance eq. 2.7 and smaller the resistance eq. 2.17. This method was proposed by Dr. Erickson in the 1990s [Eric98] and it resides in the definition of a constant relationship $R_S \cdot C_{j0}$= Const. This relationship works well between PSBDs with similar anode sizes, the same epilayer doping and the same epilayer thickness and has been successfully implemented at LERMA by Dr. A. Maestrini and Dr. J. Treuttel in frequancy multipliers [Maes03], [Maes05a], [Maes10b], [Treu16a], even up to 2.7 THz [Maes12]. It is usually considered that $R_S \cdot C_{j0}$= 120 Ω·fF if the epilayer doping is $1 \cdot 10^{17}$ cm^{-3} and the epilayer thickness is 350 nm [Eric98], [Maes10b]. However, this constant value changes if the epilayer doping or thickness change, and it can even change when using different fabrication process. The limit of this relationship is that it is necessary to have a previously fabricated PSBD with the specific doping and thickness of the epilayer to know the value of that constant relationship. This ideal assumption works better if the sizes of the anodes are much larger than the epilayer thickness, when the influence of edge effects is lower. However, it requires a large amount of experimental devices to extrapolate between PSBDs and the experience of the RF designer becomes very important at that point.

The method proposed by this author is based in the analysis proposed in [Louh95] and mostly in the results presented in Table II.2. Louhi introduces a correction factor in the resistance associated to the SC layers of the PSBD accounting for the ratio between a circular anode size, with radius r_0, and epilayer thickness W_{EP}. This model assumes a constant series resistance, as indicated by Louhi:

$$\begin{aligned} R_E &= \frac{\rho W_{EP}}{A}\gamma_r \\ \rho &= \frac{1}{qN_E\mu_E} \\ \gamma_r &\approx \left(1+\frac{4t_E}{\pi r_0}\right)^{-1}, \end{aligned} \tag{2.18}$$

where μ_E the electron mobility in the epilayer and γ_r is the correction factor due to edge effects proposed in [Louh95] for circular anodes. The correction factor proposed by Louhi describes the observed phenomena in our 2D-MC simulations. It is possible to note in Table II.2 that the series resistance is not twice bigger when the epilayer thickness is doubled.

Eq. 2.18 is used as a reference to extrapolate the series resistance $R_{S;f}$ of an hypothetical PSBD from a previous experimental PSBD known series resistance $R_{S;0}$. The correction factor given in eq. 2.18 is obtained for circular anodes while a part of our anodes is rectangular [Moro16]. However, if a circular anode surface equal to our anodes surface is supposed to calculate $r_0=(A/\pi)^{1/2}$, (2.18) is able to approximate the 2D-MC series resistances obtained for Diode1 and Diode2 in Fig. 2.6, 2.7, respectively. It slightly underestimates the Diode3 series resistance obtained with MC simulations in Fig. 2.8. However, it is not able to reproduce 2D-MC results for Diode4 and Diode5 and the predicted resistance using eq. 2.18 is much lower than predicted results by 2D-MC simulations. Nevertheless, it is not the interest of this author in this section to have an accurate analytical equation for PSBDs series resistance, but rather have an analytical equation able to correctly predict the tendency of the series resistance. This expression shows how the resistance of a PSBD depends on the epilayer thickness, the anode size, the epilayer doping and the electron mobility in the epilayers,

$$\frac{R_{S;f}}{R_{S;0}} = \left[\frac{r_{0;0}\left(\pi r_{0;0} + 4W_{EP;0}\right)}{r_{0;f}\left(\pi r_{0;f} + 4W_{EP;0}\right)}\right] \cdot \left[\frac{W_{EP;f}\left(\pi r_{0;f} + 4W_{EP;0}\right)}{W_{EP;0}\left(\pi r_{0;f} + 4W_{EP;f}\right)}\right] \cdot \left[\frac{N_{E;0} \cdot \mu_{E;0}}{N_{E;f} \cdot \mu_{E;f}}\right], \qquad (2.19)$$

where the *0*-index refers to the physical properties of the previously known PSBD and *f*-index refers to the hypothetical PSBD structure. The first factor in eq. 2.19 is associated to a change in the anode size, the second term is associated to a change in the epilayer thickness and the third term is associated to a change in the epilayer doping. μ_E is the electron mobility in the SC that can be analytically estimated using the expression described in [Schl01c]. The first and second terms are linked by the order of applications, i.e., the variation of the anode size is considered before the variation of the epilayer thickness in eq. 2.19.

However, this approximation requires some considerations when using it in PSBDs' extrapolations. This equation assumes that the external sources of resistance, like the metallic contacts, the skin effect and parasitics, change in the same way than the SC resistance associated to the epilayer. It is not true and, additionally, it is not possible to differentiate between the series resistance associated to the SCs and the external contributions. This means that a 2D-MC simulator or similar complex models are required to estimate the minimum series resistance related to the epilayer R_E in Fig. 2.4(b). It is also important to note that the correction factor given in eq. 2.18 is obtained for a circular geometry of the anode. It is therefore possible to consider that the predictions of eq. 2.19 work better if the anode size is scaled, i.e., if the contribution to the correction factor for the circular and rectangular part is maintained. A change in the epilayer doping and the epilayer thickness in eq. 2.19 can be delicate and the more differences that exist between the known PSBD and the hypothetical one, the more deviation in the predicted series resistance will be obtained. It is especially true when changing the epilayer doping because it is difficult to know the resulting modification of the epilayer mobility in real devices. Regarding the epilayer thickness contribution, it is difficult to determine since the correction factor is obtained for circular anodes. It is important to note that eq. 2.19 does not allow a change from a PSBD with hundreds of nm epilayer thickness to a new PSBD with some tens of nm. The 2D-MC simulations carried out in this section can help at this point to correctly estimate the new series resistance of the diode. It is possible to use the 2D-MC simulator to obtain a value of the series resistance for the know PSBD structure and then simulate the modified epilayer thickness to compare both resistance

values. We can assume that the experimental series resistances of those devices will feature a similar variation. Further analysis of eq. 2.19 using our 2D-MC simulator could notably improve the accuracy associated to the correction factor. However, it exceeds the theoretical analysis proposed in this dissertation. However, if the doping and thickness is not notably changed from the initial PSBD, then eq. 2.19 together with the results obtained in Table II.2 allow obtaining an adequate method to extrapolate when varying the geometry and properties of the epilayer.

2.2.3.2 The RLC Series Impedance Model

The SSEC presented in Fig. 2.4(b) proposes a RLC circuit in series configuration with the Schottky barrier junction and a series impedance associated to external impedances. The RLC circuit represents the SSEC of the SC epilayer. This equivalent circuit has provided satisfactory results in terms of MC simulations in [Gonz97]. The relationship between the lumped elements of the RLC is explained in [Gonz97], [Louh95] and their values can be obtained as:

$$\begin{cases} L_E = R_E \dfrac{m^* \mu_E}{q} \\ C_E = \dfrac{\varepsilon_{SC} \rho}{R_E} \end{cases}, \tag{2.20}$$

where m^* is the effective mass of the electrons, ρ is the resistivity of the SC, μ_E is the epilayer mobility of the electrons, q is the electrons charge and ε_{SC} is the dielectric constant of the SC. It is theoretically fulfilled the condition $L_E C_E$=const. The implementation of this model in the developed 300 GHz doubler is described in chapter 3 and in the 1.2 THz mixer in chapter 6. The external impedance in Fig. 2.4(b) has been considered as real impedance and the condition $Z_{Ext}+R_E=R_S$ has been imposed in any case. The series resistance R_S has been considered to be equally distributed between R_E and Z_{Ext}. While a small influence of the RLC model has been found in the analysis of the 300 GHz doubler, its application is useful to understand the behavior of the 1.2 THz mixer in varistor conditions along the frequency band. However, the consideration of this RLC model has not been found essential during the optimization of the different mixers since its influence on the PSBDs impedance matching is not critical.

2.2.4 Capacitance Analytical Model in PSBDs

The 2D-MC simulator has been specifically used in this work for the analysis of capacitance phenomena in PSBD structures. The capacitance behavior of SBDs below flat band conditions can be mostly associated to charge variations in the epilayer region close to the Schottky contact while additional contributions can arise when biasing the SBD above flat band conditions. The MC simulator can accurately simulate the contribution of each region of the simulated structure to the device capacitance. The well-known fringing effect has been studied using a 2D-MC simulator able to take into account two-dimensional capacitance phenomena in the proximities of the anode. A surface charge model, previously used in HEMTs simulations [Mate96], [Mate00a], [Mate00b], and explained in section 2.1.1, has been included here as a boundary condition of the epilayer-dielectric interface, used in the

passivation of the device, to study the impact on the PSBD capacitance. The fringing effect in Schottky contacts has been studied in two different cases. First, PSBD structures with thick enough epilayer thickness W_{EP} and length L_{EP} have been studied (where the full capacitance contribution comes from the charge variations within the epilayer). Second, the analysis of PSBDs with thin epilayers is performed in order to determine the influence of the substrate layer in the total capacitance of the PSBDs.

2.2.4.1 The Fringing Effect

The so-called fringing effect or "edge-effect" (EE) in PSBDs is associated to the additional depleted charge at the edge of the Schottky contact in real geometries. The 2D-MC simulated structure is illustrated in Fig. 2.2 and the depletion region profile is schematized by the dashed line. Following the previous work presented in [Louh94], the influence of surface charges placed in the dielectric-SC interface on the PSBDs capacitance has been studied by means of our 2D-MC simulator in [Moro16] (Appendix). The simulation of the PSBDs at different bias allows having the variation of charge between two simulated biases and thus, the C-V characteristic of the structure. Additionally, the 2D-MC simulator allows having the variation of charge in each single mesh of the defined structure. This has allowed studying the modifications of the depletion region profile when simulating different surface potentials in the dielectric-SC interface of the structures. The procedure and results are discussed in [Moro16] and the final analytical model of the PSBDs capacitance is expressed by:

$$C_{EE}(V_d) = A\frac{\varepsilon_{SC}}{W(V_d)} + L_{Contour}\cdot 2\varepsilon_{SC}D_1\frac{\beta(V_S)}{\beta_0} + 3\varepsilon_{SC}D_2\left[\frac{\beta(V_S)}{\beta_0}\right]^2 W(V_d)\ , \qquad (2.21)$$

with,

$$\frac{\beta(V_S)}{\beta_0} = 1 + 0.300\cdot V_S + 0.146\cdot V_S^2\ . \qquad (2.22)$$

ε_{SC} is the dielectric constant of the SC, V_S is the surface potential placed in the dielectric-SC interface, Fig. 2.2. V_S is a negative surface potential between 0 V and -0.7 V, half of the SC energy gap. The first term in eq. 2.21 is associated to the previously mentioned ideal parallel-plate capacitance of the SBDs in eq. 2.6 that emerges from the charge variation under the anode. The second term in eq. 2.21 is associated to the additional fringing capacitance, which is proportional to the length of the contour $L_{Contour}$ of the anode. It is a constant contribution independent of the epilayer properties but dependent on the anode geometry. It also depends on the EE parameter defined by Louhi in [Louh94] by $D_1 = 0.72 \equiv \beta_0$, which corresponds to the ideal case $V_S = 0$ V. We have introduced in [Moro16] a surface charge factor $\beta(V_S)/\beta_0$ based in the result of our 2D-MC simulations, which depends on the surface potential placed in the dielectric-SC interface. It is equal or lower than one and a second order polynomial matching eq. 2.22 has been used to fit the MC simulations of different PSBDs. The third term in eq. 2.21 is associated to the three dimensional contribution of circular anodes and corners of rectangular anodes and is proportional to the depletion region depth (eq. 2.4) but it does not depend on the anode geometry. The EE parameter defined by Louhi $D_2 = 0.34$ has to be corrected by the square of the surface charge factor $\beta(V_S)/\beta_0$. The correction factor associated to the surface charges $\beta(V_S)/\beta_0$ can reduce the influence of the fringing-effect up to 15 % with respect to the "classical" value of [Louh94]. The terms on D_1 and D_2 in eq. 2.21 are usually

much lower than the first term for large anodes, corresponding to capacitances of the order of some tens fF. However, the additional terms become very important as the anode surface is reduced. This is due to the contribution of the term on D_1 that decreases as the square root of the anode surface, and the term on D_2 that remains constant.

2.2.4.2 The Substrate Effect

The second study of the depletion region behavior has been carried out when substantially reducing the epilayer thickness. The extension of the depletion region generated by the anode into the region surrounding the epilayer-substrate interface produces an inhomogeneity in the depletion of the epilayer charge. The objective of this section is defining an analytical equation that approximates the impact of the substrate layer on the PSBD capacitance to develop the so-called substrate-effect (SE) model. The mentioned phenomenon has been schematized in Fig. 2.11, where it is possible to observe two different PSBD structures equally biased with the same physical properties and geometry, but presenting a different epilayer thicknesses. According to Fig. 2.11(b), the vertical depletion region depth is expected to be substantially reduced due to the proximity of the substrate which features a higher electron concentration. Additionally, the horizontal depletion depth associated to the fringing effect is the same in both cases due to the homogenous concentration of the epilayer in that direction.

Two different analyses are required here to differentiate the influence of the substrate on the vertical and horizontal depletion region depths. A one-dimensional analysis is performed first in order to isolate the influence of the substrate on the depletion region depth. Results obtained from the one-dimensional analysis are secondly applied to the 2D-MC simulations of PSBD structures to determine the combined interaction of the substrate and the fringing effect.

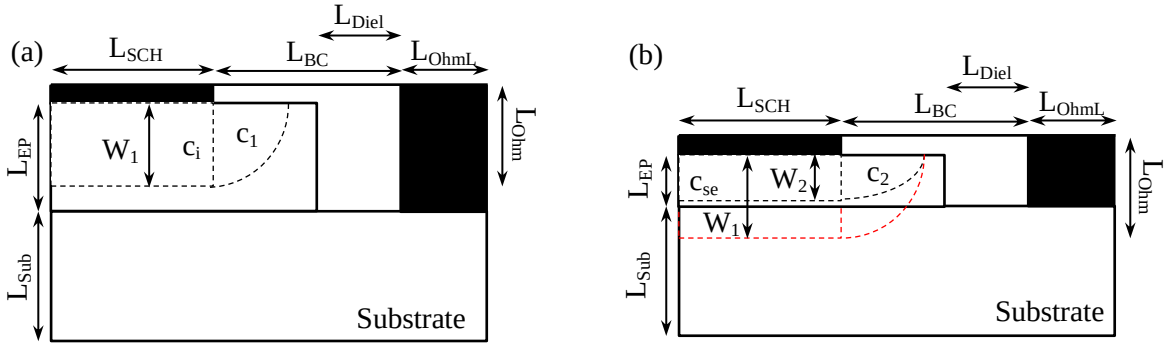

Fig. 2.11. Scheme of a 2D-MC PSBD simulated structure when considering (a) a thick and (b) thin epilayer thickness in the same structure. The depletion region profile when reverse-biasing the diode is illustrated by the dashed black line in both figures. The dashed red line in (b) illustrates the case shown in (a) when no influence of the substrate is observed.

A. One-Dimensional Monte Carlo Approach

A one-dimensional structure has been simulated in this case consisting of an epilayer of 80 nm and a substrate layer of 90 nm. The capacitance of the defined SBD structure is calculated as explained in [Moro16]. The variation of the average number of particles in the Monte Carlo simulation in bias steps of 0.5 V at high reverse bias and 0.05 at bias close to flat band is

monitored to calculate the capacitance. The capacitance characteristics obtained when varying the simulated epilayer doping are plotted in Fig. 2.12.

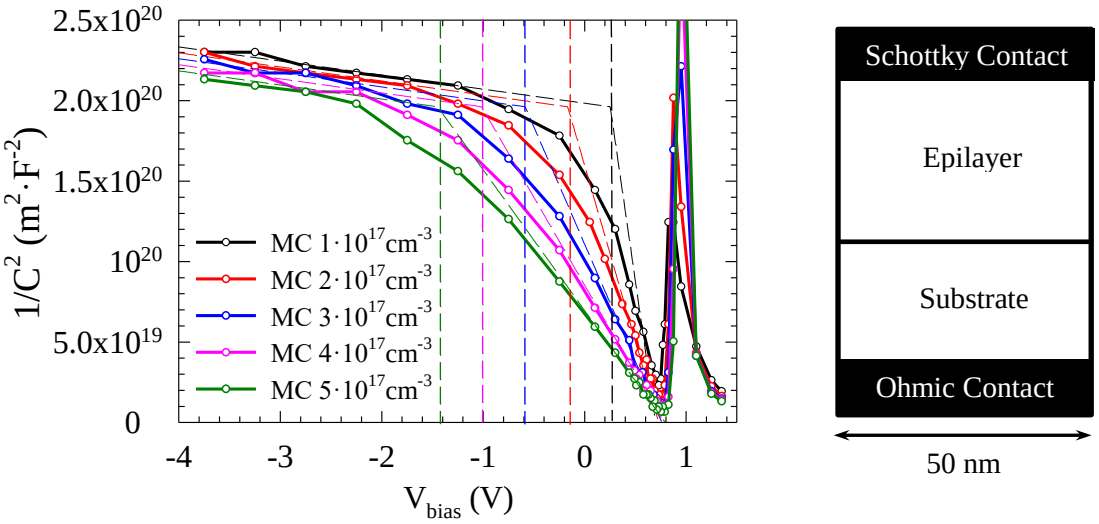

Fig. 2.12. Capacitance obtained with the MC simulations (dotted solid lines) of a 80 nm epilayer with different doping levels from $1{\cdot}10^{17}$ to $5{\cdot}10^{17}$cm^{-3} and a substrate doped at $5{\cdot}10^{18}$cm^{-3}. The MC results are compared with the capacitance associated to an ideal abrupt doping transition of the electron concentration (dashed lines), eq. 2.25. The vertical dashed lines correspond to the bias point for which the depletion region reaches the transition (using eq. 2.4, $W(V)= W_{EP}$).

These results are compared with the ideal capacitance given by equation eq. 2.6 per unit surface associated to an abrupt doping transition between the epilayer and the substrate. It is possible to define the bias $V_d=V_{EP}$, that corresponds to a fully depleted epilayer in accordance with eq. 2.4, illustrated by dashed vertical lines in the figure for each epilayer doping. The ideal SBD capacitance for an abrupt transition can be calculated as:

$$c(V_d) = \begin{cases} \sqrt{\dfrac{q\varepsilon_{sc}}{2}} \dfrac{1}{\sqrt{\dfrac{(V_B - V_d)}{N_E}}} & if \quad V > V_{EP} \\ \sqrt{\dfrac{q\varepsilon_{sc}}{2}} \dfrac{1}{\sqrt{\dfrac{(V_B - V_{EP})}{N_E} + \dfrac{(V_{EP} - V_d)}{N_S}}} & if \quad V < V_{EP} \end{cases} . \tag{2.23}$$

where N_S is the substrate doping. It is possible to note in Fig. 2.12 that eq. 2.23 fits the MC results at biases close to flat band conditions and at strong reverse bias conditions. However, the MC simulations of the structure show a gradual transition from the ideal C-V dependence of the epilayer to the one of the substrate. It is worth noting in Fig. 2.12 that the MC results start deviating from the value expected from eq. 2.6 at reverse biases lower than V_{EP}. This is because the epilayer-substrate interface does not produce an abrupt transition of the electron concentration. It is possible to define the critical voltage value V_{CA} associated to the depletion region depth $W(V_{CA})= W_{CA}< W_{EP}$ that defines the point from which eq. 2.23 does not fit MC results. The approach proposed by this author to obtain the depletion region depth from MC results consists in considering that the capacitance of the simulated SBD structure is still described by equation eq. 2.6. However, the depletion depth does not follow the ideal behavior described by the total depletion approximation given by equation (2.4). We have

calculated the depletion region depth W in the simulated structure by using (2.6) with the capacitance results obtained with the MC simulations (presented in Fig. 2.12). The depletion region depth associated to the simulated structure when varying the epilayer doping is plotted in Fig. 2.13.

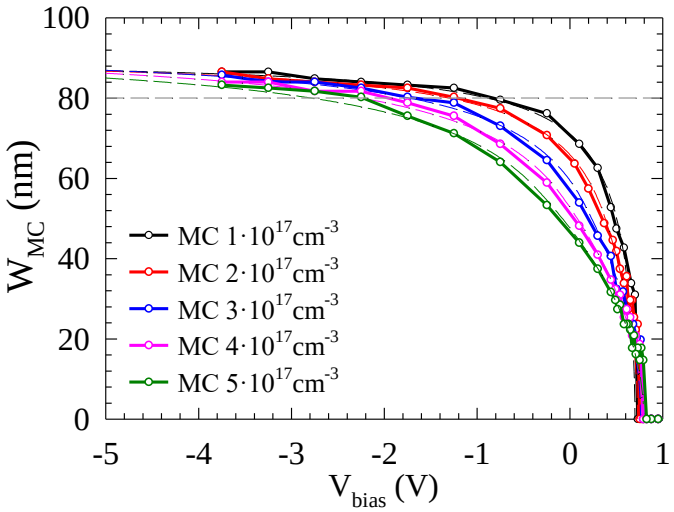

Fig. 2.13. Depletion region depth obtained from the MC simulations compared with the analytical capacitance model given by eq. 2.24 accounting for the substrate effect (dashed lines). The 80 nm epilayer thickness is illustrated by the dashed grey line.

It is possible to note in Fig. 2.13 that the depletion region depth at high reverse-bias tends to a similar value in all simulated cases of epilayer doping. The depletion region depth increases fast as the reverse bias increases and the epilayer is depleted but it is held by the substrate due to the much higher electron concentration in this SC layer. MC results plotted in Fig. 2.13 indicate that the depletion region cannot enter more than a few nm into the substrate layer. This allows to define a two-parameters analytical model based in the critical bias point when the C-V characteristic starts to deviate from the ideal value $W(V_{CA})=W_{CA} < W_{EP}$ and the asymptote point $W_{CB} > W_{EP}$. The considered analytical function is given by:

$$W^2(V_d) = \begin{cases} W_1^2(V_d) = \dfrac{2\varepsilon_{SC}}{qN_E}(V_B - V_d) \quad at \quad V_d \geq V_{CA} \\ W_2^2(V_d) = W_{CB}^2 - \dfrac{(W_{CB}^2 - W_{CA}^2)^2}{(W_1^2(V_d) - W_{CA}^2) + (W_{CB}^2 - W_{CA}^2)} \quad at \;\; V_d \leq V_{CA} \end{cases}, \qquad (2.24)$$

where the depletion region $W_1(V_d)$ is equivalent to that one given by eq. 2.4 when $V_d \geq V_{CA}$ but its behavior is given by $W_2(V_d)$ when $V_d \leq V_{CA}$. The continuity of the function and the derivate in $V_d = V_{CA}$ has been imposed between $W_1(V_d)$ and $W_2(V_d)$. The values of the parameters W_{CB} - W_{EP} and W_{EP} - W_{CA} used to fit the MC results in Fig. 2.13 using eq. 2.24 are indicated in Table II.3.

Using the value of the bias dependent depletion depth given by eq. 2.24 in eq. 2.6 it is possible to define the capacitance of a one-dimensional SBD accounting for the substrate effect. Eq. 2.24 assumes an asymptotic behavior of the depletion region at $W(-\infty) = W_{CB}$ which is not real. However, this analytical approximation of the depletion region depth is enough to correctly fit the 2D-MC results in the voltage range typically used in the experimental modules developed within this work and in other practical applications. PSBDs for mixing applications are normally excited with a time-dependent voltage signal that oscillates between

-1 and 1 V while for frequency multiplication one usually avoids to have such thin epilayer thicknesses because the SE degrades the efficiency of harmonic generation [Sile11a].

N_E (cm^{-3})	N_S (cm^{-3})	W_{EP}-W_{CA} (nm)	W_{CB}-W_{EP} (nm)
$1 \cdot 10^{17}$	$5 \cdot 10^{18}$	46	10
$2 \cdot 10^{17}$	$5 \cdot 10^{18}$	30	11
$3 \cdot 10^{17}$	$5 \cdot 10^{18}$	26	13
$4 \cdot 10^{17}$	$5 \cdot 10^{18}$	24	14
$5 \cdot 10^{17}$	$5 \cdot 10^{18}$	22	14

Table II.3. Values of W_{CA} and W_{CB} used in (2.26) to fit results presented in Fig. 2.13.

B. Two-Dimensional Monte Carlo Approach

Once an analytical model of the vertical depletion region depth accounting for the substrate effect has been developed, we focus the analysis on the interaction between the substrate effect and the fringing effect. The 2D-MC Diode4 structure defined in Table II.1 has been simulated for two different epilayer thickness, 55 nm and 180 nm, without considering any surface charge (V_S= 0 V). The electron concentration in the full simulated structure at V_d=V_{bias}= -1 V for both epilayer thicknesses has been plotted in Fig. 2.14. The different layers of the simulated structure are indicated. The green region is the non-depleted epilayer zone at equilibrium, where the electron concentration equals the doping at $3 \cdot 10^{17}$ cm^{-3}, while the red regions are depleted. The violet region corresponds to the substrate and the epilayer-substrate interface marked by a dashed white line.

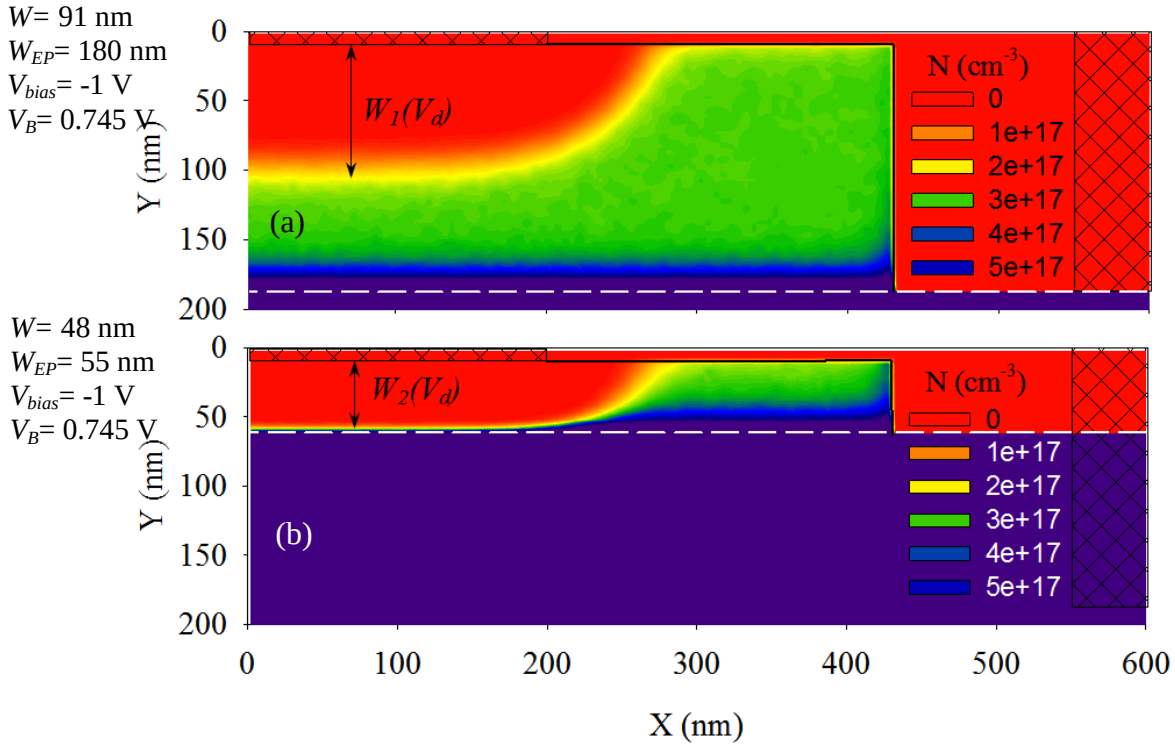

Fig. 2.14. Electron concentration obtained with the 2D-MC Diode4 structure when simulating (a) 180 nm and (b) 55 nm epilayer thickness at V_{bias}= -1 V.

The only difference between Fig. 2.14(a) and (b) is the simulated epilayer thickness. It is possible here to note the reduced depletion region depth in Fig. 2.14(b) as compared to Fig.

2.14(a) due to the presence of the substrate layer. The vertical depletion region in both cases can be described by eq. 2.24. The horizontal extension of the depletion region at the edge of the Schottky contact is shown to be the same in both cases, but the shape of this additional depleted region has been modified by the proximity of the substrate. It is important to note that the horizontal depth of the additional depletion region is linked to the vertical depletion region depth, defined by W_1 in eq. 2.24 by the Poisson equation resolution, even if the substrate modifies the vertical depletion region. We propose to quantify this modification following the scheme shown in Fig. 2.11, where two different capacitance contributions from the additional depletion region at the edge of the anode will be considered, c_1 and c_2, corresponding to the calculation without and with substrate effect, respectively. The capacitance per unit length value c_1 is given by the second term of eq. 2.21.

This author proposes to fit the additional depletion region border of both c_1 and c_2 regions with an analytical equation described by $f(x,V)=[(x- B(V_d))/A(V_d)]^{1/n}$ where $A(V_d)$ and $B(V_d)$ are fitting parameters which depend on the bias. It is possible to adjust the shape of the region described by this equation with the n exponent. This equation allows calculating the surface A_1 and A_2 contained in regions c_1 and c_2, respectively. Then, assuming a substrate doping much higher than the epilayer, the quotient between A_1 and A_2 is equal to the quotient of the capacitances, since the charge within those regions can be obtained as the multiplication of the surface by qN_E, (as long as the depletion region does not enter into the substrate layer, which is not a bad approximation since the N_S is usually much higher than N_E). Assuming that both depletion regions c_1 and c_2 can fit with the same n factor, the relationship between the known capacitance without SE and the unknown capacitance with SE can be approximated by:

$$\Gamma_S(V_d) = \frac{A_2}{A_1} = \frac{\beta(V_S)W_1(V_d)W_2(V_d)\frac{n}{n+1}}{\beta(V_S)W_1^2(V_d)\frac{n}{n+1}} = \frac{c_2}{c_1} = \frac{W_2(V_d)}{W_1(V_d)} \leq 1 \ . \tag{2.25}$$

Eq. 2.25 defines the SE correction factor required to modify the second term in eq. 2.21 in order to account for the substrate effect influence on the additional depletion region in rectangular anodes. This factor is just the ratio between the depth of the real depletion region that can be obtained with eq. 2.24 and the ideal value, eq. 2.4, obtained for an infinitely thick epilayer. The square value of this correction factor has also to be included in the third term of eq. 2.21. $\Gamma_S(V_d)=1$ if the depletion region does not exceed $W(V_{CA})= W_{CA}$. The modification of eq. 2.21 required to account for the SE if $V_d < V_{CA}$ is finally given by,

$$C_{SE}(V_d) = A\frac{\varepsilon_{SC}}{W_2(V_d)} + L_{Contour}\cdot 2\varepsilon_{SC}D_1\frac{\beta(V_S)}{\beta_0}\Gamma_S(V_d) + 3\varepsilon_{SC}D_2\left[\frac{\beta(V_S)}{\beta_0}\Gamma_S(V_d)\right]^2 W_1(V_d) \ . \tag{2.26}$$

The depletion region depth behavior described by W_2 in eq. 2.26 is used in the first term of eq. 2.28 to account for the depleted charge under the anode. The SE correction factor is used in the second term of eq. 2.26 to account for the reduction of depleted charge at the edge of the anode. The square of the SE correction factor is included in the third term of eq. 2.26 for the same reason that the square of the EE correction factor $\beta(V_S)/\beta_0$, but this still uses the depletion region depth dependency given by W_1 in eq. 2.26 for all the values of V_d. It is

because the horizontal depth of the additional depletion region remains constant, thus the radial integration limit is defined by W_1 instead of W_2. Eq. 2.26 is equivalent to eq. 2.24 if $V_d > V_{CA}$ since $\Gamma_S(V_d)= 1$ and $W_2(V_d)=W_1(V_d)$.

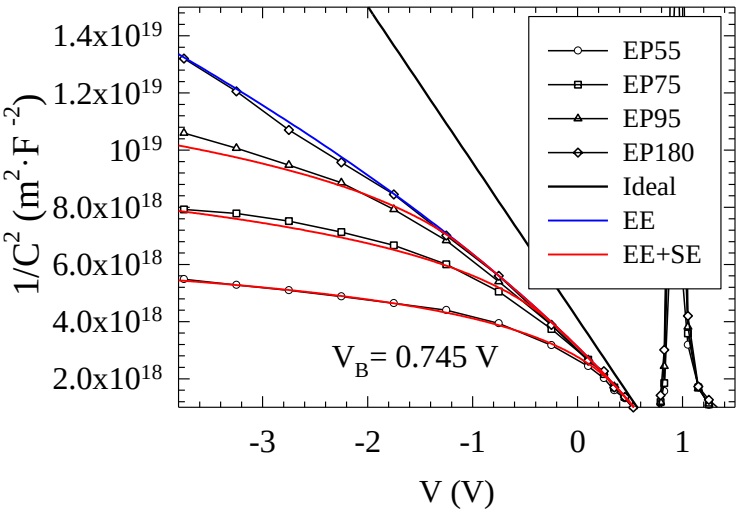

Fig. 2.15. 2D-MC capacitance results of Diode4 structure when simulating a 55 nm, 75 nm, 95 nm and 180 nm epilayer thicknesses. The MC results have been fitted using eq. 2.8 (red lines) and eq. 2.6 (blue line) capacitance model.

Finally, it is possible to fit the 2D-MC results of Diode4 structure using eq. 2.21 and eq. 2.26. The third term of these equations is not accounted for in Fig. 2.15 since the 2D-MC simulator does not have that influence. The capacitance $1/C^2$ obtained in MC simulations of Diode4 when reducing the epilayer thickness is plotted in Fig. 2.15. The MC capacitance results obtained with the epilayer thicknesses, W_{EP}, at 55, 75 and 95 require to be fitted by eq. 2.26 while the case W_{EP}= 180 nm can be fitted with eq. 2.4. Values for W_{EP} - W_{CA} = 23 nm and W_{CB} – W_{EP} = 11 nm have been used in all cases obtaining satisfactory results on the epilayer thickness dependence described by eq. 2.26.

A. Generalization of the Capacitance Model

The developed analytical model described by eq. 2.24 and 2.26 is able to account for both the edge effects, associated to 2D and 3D fringing capacitances, and the substrate effect. This model has been developed by using our 2D-MC simulator using a fixed substrate doping that has led to the SE parameters described in Table II.3. However, the values of these parameters change if the substrate doping is modified and the validity of Table II.3 cannot be assured. In fact, MC simulations of every case should be made in order to have an accurate determination of those parameters. However, a simple approximation for the value of W_{EP} - W_{CA} is the ideal length of the space charge region of an asymmetric p^+-n junction [Sze06], given by,

$$W_{EP} - W_{CA} \approx \sqrt{\frac{2\varepsilon_{SC}\varphi_j}{qN_E}} \quad , \tag{2.27}$$

where φ_j is the built-in voltage of the epilayer-substrate junction. The higher the difference between N_E and N_S is, the better the approximation given by eq. 2.27. The built-in voltage φ_j of the junction can be approximated using eq. 2.13 for both the epilayer and the substrate in

order to know the distance between the bottom of the conduction band at each side of the epilayer-substrate junction.

Regarding W_{CB} - W_{EP}, it is not possible to provide a simple analytical approximation and a solution for the Poisson equation accounting for the SC degeneracy is required for any combination of the epilayer and substrate doping. A reasonable approximation to define an adequate value of W_{CB} - W_{EP} in the SE model given by eq. 2.24 and 2.26 is comparing this model with the abrupt approximation in eq. 2.23 for a fixed W_{EP} - W_{CA} value. Once W_{EP} - W_{CA} is defined in eq. 2.26, it is necessary to define the value W_{CB} - W_{EP} that makes eq. 2.26 to fit the capacitance defined by an abrupt doping discontinuity described by eq. 2.23.

2.3 The Analytical Model in Harmonic Balance Simulations

The implementation of the analytical models in the electrical model of SBDs used in ADS simulations is discussed in this section. An electrical model of SBDs is already implemented in the ADS software and it is widely used by RF engineers. This is the reason for the so-called "Standard" (STD) model defined in this work to indicate that the already included ADS electrical model for SBDs is used. Another component available in ADS simulations is the so-called Symbolically Defined Device (SDD). These SDDs allow defining an element with a number *n* of ports in which it is possible to define an analytical relationship between the voltage and the current in each port. It is also possible to define a relationship between the current and the derivate of a time-dependent voltage signal in each port. The modifications of the capacitance model developed in section 2.2.4 have been implemented in ADS simulations using a 2-port SDD element to define the conduction and induction currents in the PSBD electrical model.

A. The STD Model of SBDs in ADS Simulations

The standard model in ADS simulations is a general model of diodes that can be implemented in different kind of these devices. The equations used in this work when considering the STD model of SBDs are shown in Table II.4. This model is based on the SSEC shown in Fig. 2.4(a). It is important to note that the definition of the voltage in this section includes both the bias supply and any time-dependent voltage, $V= V_{bias}+V(t)$, between the pins of the SBD circuit element defined in ADS. A new parameter $\alpha \leq 1$ is defined in the STD model to differentiate two voltage ranges, $V \leq \alpha V_B$ and $V>\alpha V_B$. This parameter is a widespread technique used in diodes modeling to avoid the pole of the capacitance analytical equation eq. 2.6 at $V=V_B$. The α parameter defines the point αV_B from which the C-V characteristic definition is modified by other analytical equation without any pole. The implemented analytical equation in the STD model at $V \geq \alpha V_B$ defines a linear function. The condition of continuity of the function and the first derivate is imposed between eq. 2.6 and the linear equation. This is required by the ADS simulator since the harmonic balance solver uses Newtonian numerical methods in which the continuity of the functions is required for the convergence of the solutions. The *M* parameter is associated to the doping distribution in the epilayer. Different values of *M* allow considering a gradient in the doping of the epilayer. M=1/2 is used in this work and it means that a homogeneous doping distribution of the epilayer is considered.

STD diode model	$V< \alpha V_B$	$V> \alpha V_B$
I-V	$I_S(e^{\frac{qV}{\eta KT}}-1)$	$I_S(e^{\frac{qV}{\eta KT}}-1)$
C-V	$\frac{C_{j0}}{\left(1-\frac{V}{V_B}\right)^M}$	$\frac{C_{j0}}{(1-\alpha)^M}\left[1+\frac{M}{V_B(1-\alpha)}(V-\alpha V_B)\right]$

Table II.4. I-V and C-V equations defined in the ADS standard diode model.

The current transport is defined by eq. 2.15 for all considered voltage values. The STD model only requires the definition of I_S and η. The constant series resistance R_S is simulated as indicated by the SSEC in Fig. 2.4(a). It is important to note that the STD model in ADS is not defined to consider any temperature other than T= 295 K because KT=0.0254 V is intrinsically defined in ADS simulations. The only way to modify the temperature of the simulated STD model is correcting the defined ideality factor by $\eta' = \eta \cdot T/295$ where η is the considered value at temperature T. Regarding the capacitance equation, it is necessary to define the value of the junction capacitance C(0)= C_{j0}, M, α and the built-in voltage V_B. The capacitance model does not consider any geometry of the anode and the value of C_{j0} has to be externally calculated by the user. Additionally, the capacitance equation in the STD model does not take into account the modification introduced by the fringing effect and it considers a linear behavior of $1/C^2$. The fringing effect has been approximated by some authors in [Maes05a], [Maes06b], [Maes10b], [Maes12], [Treu14], [Treu16a] by calculating C_{j0} as mentioned in [Louh94].

B. The SDD Model of PSBDs in ADS Simulations

The SDD model has been defined with the improved capacitance model developed by this author and presented in section 2.2. The equations used in this work when considering the SDD model of SBDs are shown in Table II.5 for the case $V< \alpha V_B$ and $V_{CA}< \alpha V_B$.

SDD diode model	$V_{CA} \leq V \leq \alpha V_B$	$V \leq V_{CA}$ & $V_{CA} < \alpha V_B$
I-V	$AJ_S(e^{\frac{qV}{\eta KT}}-1)$	$AJ_S(e^{\frac{qV}{\eta KT}}-1)$
C-V	Eq. (2.23)	Eq. (2.28)

Table II.5. I-V and C-V equations defined in the new SDD model of the Schottky diode.

Two different cases appears now for $V> \alpha V_B$. The first case fulfill the condition $V_{CA}< \alpha V_B$ when $V> \alpha V_B$ and the linear capacitance is described by,

$$C_{EE}(V) = \frac{C_{j0}}{2\sqrt{1-\alpha}}\left[\frac{1}{1-\alpha} - A3D_2\left[\frac{\beta(V_S)}{\beta_0}\right]^2\frac{\varepsilon_{SC}^2}{C_{j0}^2}\right]\left(\frac{V}{V_B} - \alpha\right) + C_{EE}(\alpha V_B)\ . \qquad (2.28)$$

The second case fulfill the condition $V_{CA}> \alpha V_B$ when $V> \alpha V_B$ and the linear capacitance is described by,

$$C_{SE}(V)=\frac{A^2\varepsilon_{SC}^3}{2C_{j0}^2W_2(\alpha V_B)}\left[\left(\frac{A}{W_2^2(\alpha V_B)}-6D_2\left[\frac{\beta(V_S)}{\beta_0}\right]^2\Gamma_S(\alpha V_B)\right)\frac{(W_{CB}^2-W_{CA}^2)^2}{[(W_1^2(\alpha V_B)-W_{CA}^2)+(W_{CB}^2-W_{CA}^2)]^2}\right.$$
$$\left.+3D_2\left(\frac{\beta(V_S)}{\beta_0}\right)^2\Gamma_S^3(\alpha V_B)\right]\left(\frac{V}{V_B}-\alpha\right)+C_{SE}(\alpha V_B)\quad . \tag{2.29}$$

Eq. 2.29 is usually required during the simulation of PSBDs in the SDD model while eq. 2.29 will only be required in the PSBDs with the epilayer thickness dramatically reduced. Eq. 2.20, 2.29 and Table II.5 define the set of analytical equations used in the SDD model to define the electrical behavior of the PSBDs.

The SDD model has been used in this work to analyze the experimental performances of frequency multipliers in Chapters 3 and 4 in accordance with the PSBDs properties. It has also been used to analyze the performances of frequency mixers in Chapters 5 and 6. Two different test benches have been defined by this author in ADS simulations in order to analyze the potential performances of specific PSBDs for frequency doublers and frequency mixers.

2.3.1 Single Varactor PSBD Simulations for Doublers

The approach proposed in this section has been used to study the potential performance of PSBDs in frequency doubler applications using the ADS test bench shown in Fig. 2.16. This test bench consists of a single PSBD defined with the developed SDD model using the SSEC presented in Fig. 2.4(a). The PSBD is pumped by a single LO signal generated by a one-tone time-domain signal ADS element. The one-tone source provides the first harmonic at $f_1=f_{LO}$ and the defined LO power. The LO source features an impedance and it is isolated from the PSBD response using an ideal pass-band filter defined with a one-port S-parameter ADS element. The second harmonic is also extracted from the PSBD response using an ideal pass-band filter at $f_2=2f_1$ and delivered into an output load used to match the PSBD second harmonic. The upper harmonics of the PSBD response are extracted by an ideal high-pass filter and delivered to a 50 Ω load. These separated paths of each harmonic allows the LO source impedance and the output load to interact uniquely with the first and second harmonic of the PSBD response, respectively. A DC power supply is defined to bias the PSBD. The bias supply allows tuning the PSBD to improve the coupling with the LO input signal and the second harmonic generation efficiency. The defined bias supply is prevented from entering into the ideal filters using a DC blocker. The potential performance of a specific PSBD defined with the developed SDD model can be analyzed in accordance with the available LO power and the required LO frequency range. The procedure followed by this author consists of an optimization of the second harmonic generation efficiency of the PSBD and the bias supply for a specific LO power and LO frequency. The second harmonic generation efficiency of the PSBD is defined as the quotient between the generated output power at the second harmonic and the coupled LO input power. The optimization of the PSBD response is accomplished by optimizing the impedance of the LO source and the second harmonic load together with the bias supply to match the PSBD with the input LO signal and the output load. The second harmonic generation efficiency and LO and output load impedances are monitored to determine the maximal conversion efficiency of the defined PSBDs. This process must be carried out for each considered LO input power and LO frequency delivered by the simulated LO source.

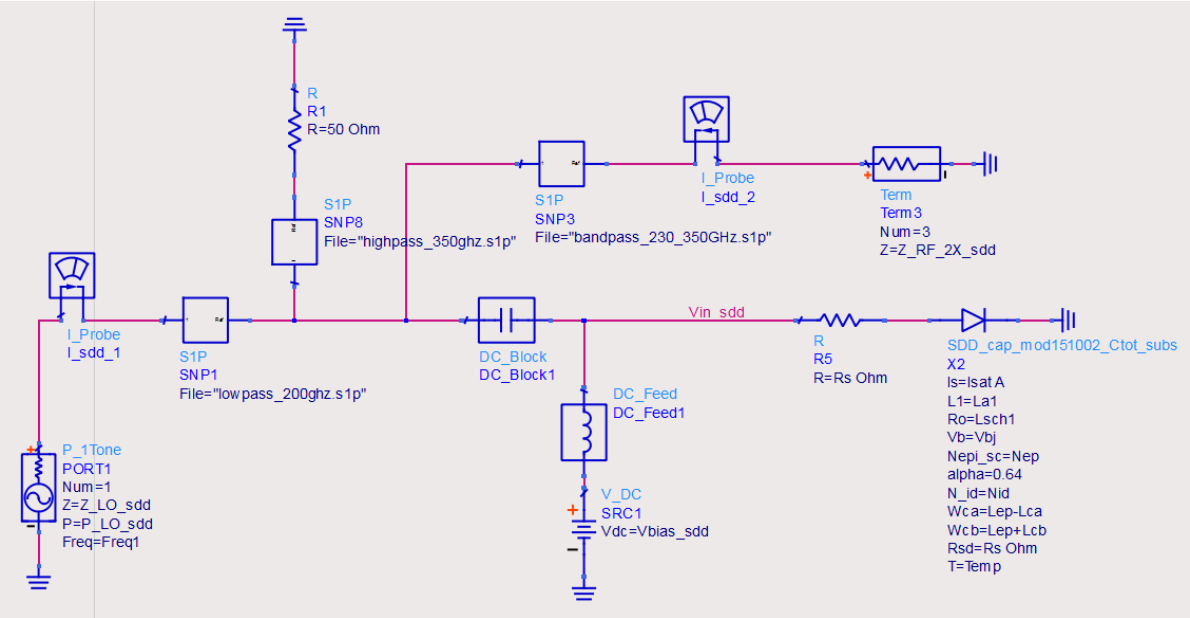

Fig. 2.16. ADS test bench defined to analyze the performances of PSBDs in frequency doublers. The different elements of the non-linear circuit are indicated.

This iterative optimization of the PSBD optimal response at each frequency is required to emulate the matching network system defined in later stages of the doubler design. The matching network consists of waveguides and transmission lines that will be optimized to match the PSBDs as much as possible along the frequency band. It is important to note that the test bench defined in Fig. 2.16 allows ideally matching the PSBD for both the input LO and output second harmonic impedances. This is not a real approach since the real matching network capabilities will be reduced as the required frequency range increases. This means that analysis of the PSBD response stability along the considered frequency range must be carried out to determine the most suitable PSBD properties. This approach will be implemented in Chapter 4 to find the suitable properties of PSBDs for a 600 GHz doubler between 270 GHz and 320 GHz.

2.3.2 Antiparallel Varistor PSBDs Simulations for Mixers

This is an equivalent approach to the analysis shown in Fig. 2.16, but some additional requirements have to be accounted for to analyze the potential performance of PSBDs in mixing applications. The most important point in subharmonic frequency mixer applications based in an antiparallel configuration of the PSBDs is the intimate dependence of the IF signal generation efficiency on this configuration of the diodes. The antiparallel configuration of the PSBDs is used to confine the even harmonics of the input LO signal. The odd IF intermodulation product at frequency $f_{IF}=nf_{LO}\pm f_{RF}$ comes out of the antiparallel configuration for all even values of n. This means that the generation of the IF signal when mixing the RF signal with one of the even harmonics of the LO singal depends on how the considered LO even harmonic is confined. This is the reason for the simulation of two PSBDs in antiparallel configuration that is required in the ADS test bench shown in Fig. 2.17. This test bench is dedicated to the analysis of subharmonic mixer with $f_{IF}=2f_{LO}\pm f_{RF}$. The simulation of two PSBDs allows defining the confinement of the desired LO even harmonic. A bias source is defined in this test bench and the DC blockers are used to define the PSBDs in series

configuration with respect the DC path. This bias supply is useful for mixing applications in which there is not enough LO power to pump the diodes. Two different one-tone sources are defined in the ADS test bench for both the LO and the RF input signals. An impedance is defined for each signal source and isolated from the diode cell response using ideal band-pass filters. The IF intermodulation product at frequency f_{IF} is now extracted using an ideal low-pass filter that delivers the desired signal into a 250 Ω load. The low-pass filter is defined up to 80 GHz to allow the transmission of upper harmonics of the IF signal at frequencies $2f_{IF}$, $3f_{IF}$, etc. These upper harmonics appear from upper intermodulation products of the LO and RF signals and two upper harmonics of the IF signal must be considered to ensure the convergence of the simulated response at the desired IF frequency signal. All the frequency signals higher than the RF signal frequency range are extracted by an ideal high-pass filter and delivered into a 50 Ω load. The impact of the third LO harmonic in the RF generation will be analyzed in Chapter 5 and 6.

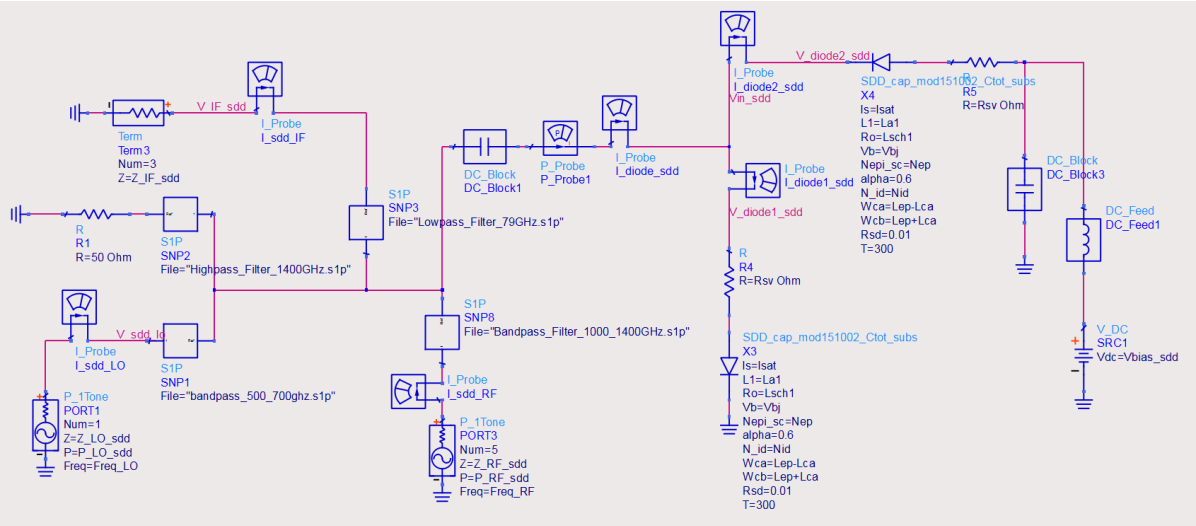

Fig. 2.17. ADS test bench defined to analyze the performances of PSBDs in antiparallel configuration for subharmonic mixers. The different elements of the non-linear circuit are indicated.

The fixed IF impedance value at 250 Ω has been considered in this case. The IF impedance is used to define the matching network conditions that must be fulfilled by both the LO and the RF signals to generate the adequate IF signal. It has been observed during this work that the higher the IF impedance, the higher the IF generation efficiency for any considered PSBD. However, the generated IF signal must be extracted from the real module through a connector that is usually standardized at 50 Ω. This means that these kinds of modules require an adapter circuit if an IF impedance load different of 50 Ω is considered. The higher the difference between the impedances matched by the adapter circuit, the higher the losses of the IF signal. The considered 250 Ω value is a trade-off between the improvement of the IF generation efficiency and the capabilities to design an adapter circuit at the IF frequency range.

The optimization of the IF generation is much more complex for frequency mixers than for frequency doublers. The most important point in frequency mixer design is the coupling of the RF signal with the PSBDs. However, it is required to pump the diode cell with enough LO power to get the diodes sensitive to the RF signal. Each considered set of properties for a

PSBD features an optimal LO input power to perform the highest sensitivity to the RF signal. This optimal situation can be achieved when there is not a limitation in the available LO input power. However, this optimal situation is very difficult to obtain when being limited by the available LO input power and a bias supply can be used to mitigate the impact of this limited power in the mixer performance. This is because the LO and the RF matching network of these modules are defined by common structures of the microelectronic chip which makes it difficult to perform both a high RF coupling efficiency and an optimal LO coupled power. The GaAs-PSBD-based mixers used in this work require at least 300-400 μW of LO power per diode to perform correctly. This means that an input LO power of at least 600-800 μW is required coupled with the diode cell in addition to the LO power lost in the matching network system. The ADS test bench shown in Fig. 2.17 highlights the required LO power for a specific mixing application. This approach is implemented in Chapters 5 and 6 to analyze the potential performance of different sets of PSBDs in the required frequency range.

2.4 Conclusions

The analytical current and capacitance equations of the PSBDs electrical model have been reviewed in this chapter using a 2D MC simulator as reference. The considered expression for PSBDs current model in this work have been compared with other authors bibliography, and the capacitance model has been extended accounting for the surface charges in the proximities of the Schottky anode. Two different SSEC based in the LEC model have been presented in this chapter accounting for the resistivity of the diode. This has led to a proposed analytical equation for the extrapolation of the resistance in different PSBD structures, which can be further extended using the 2D MC simulator. Finally, the implementation of this analytical model in non-linear HB simulator (ADS) has been carried out and used along this work. The influence of the extended SDD model on the predicted performance of the different developed modules will be compared in different chapters. Additionally, the presented SSEC model will be compared in different chapters to conclude the usefulness in the design of Schottky-based doublers and mixers modules.

Part 2: The JUICE-SWI Project

3 A Power-combined 300 GHz Frequency Doubler

The development of a 300 GHz frequency doubler is presented in this chapter. The development of this device was proposed by Dr. J. Treuttel before the beginning of this doctoral work within the framework of the JUICE-SWI project, specifically for the LO source at 270-320 GHz necessary for the 600 GHz channel of the SWI instrument. The design of the 300 GHz MMIC doubler chip is briefly described in this chapter since its conceptual development and fabrication technique is discussed in [Treut14] and the final device performance is presented in [Treut16]. However, modifications introduced in the design of a power combine 300 GHz doubler are detailed in this section as well as in the experimental results. Finally, results of the experimental I-V characteristics are used in ADS-HFSS simulations, where the physical model developed in Chapter 2 of this work is discussed and compared with the standard model (Section 2.3) to analyze its prediction capabilities.

3.1 The 300 GHz Frequency Doubler Chip

3.1.1 Description of the Virtual Device

This multiplier, shown in Fig. 3.1, features an anti-series set of four planar Schottky diodes integrated within the suspended microstrip circuit on a 4 µm-thick GaAs membrane placed in a split mechanical block by metallic beam-leads. The diodes are in a balanced configuration in a way that the odd harmonics are generated in opposite phase by each branch of the diode cell while the even harmonics are generated in phase. This results in odd harmonics cancellation leading to a simpler and more compact design where only even harmonics are propagated in the chip.

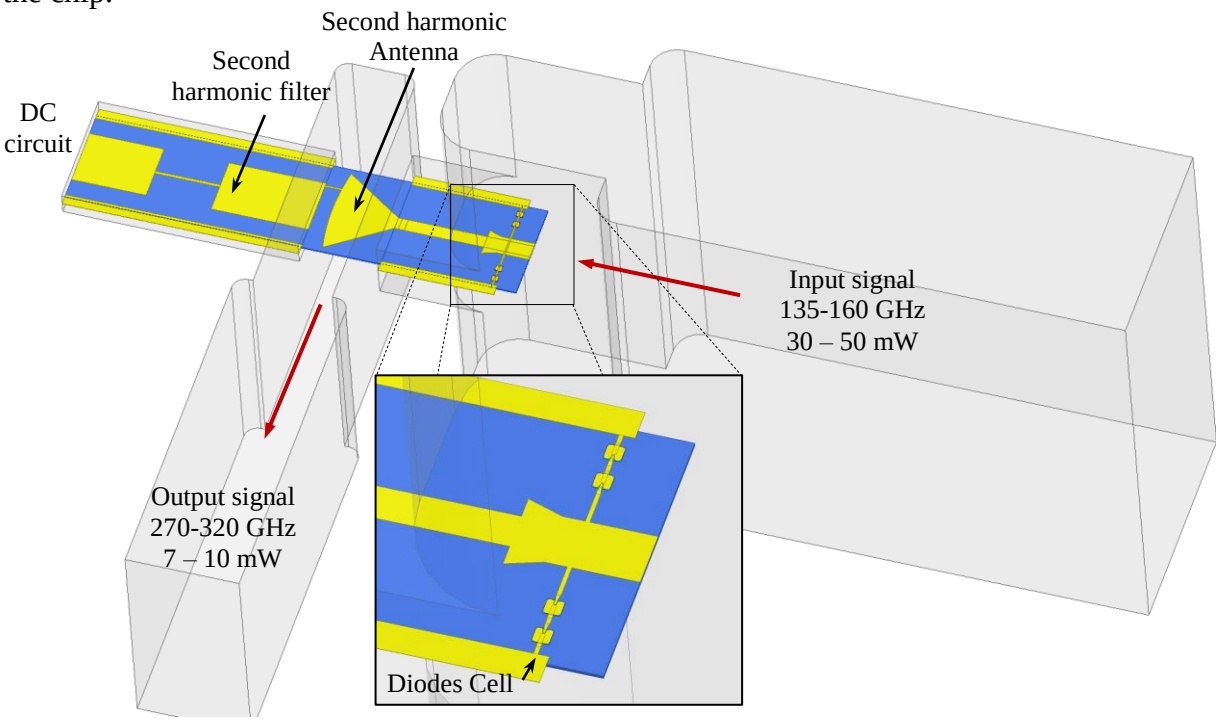

Fig. 3.1. LERMA's HFSS 3D design of the 300 GHz frequency doubler where the different parts of the MMIC chip are indicated. A balanced configuration of Schottky diodes is specially remarked.

The input LO signal which reaches the MMIC chip is led by waveguides in which the height is specifically designed to transmit the TE_{10} mode at the input frequency signal range and cut off the TM_{11} mode for avoiding losses and improving the LO coupling. The input structure of the device is designed for coupling the diodes cell with the TE_{10} mode transmitted within the input waveguide. The generated odd harmonics cancel each other out in the diode cell while the even harmonics are propagated in a quasi TEM transmission line mode to the output stage of the MMIC chip. An intermediate coplanar transmission line connects the input and output waveguides matching network. The size of the waveguide section that reach the chip is designed to match the diodes cell impedance and to cut off the upper propagation modes that could be coupled with the second harmonic generated by the diodes. A high-low transmission line filter optimized for cutting off the second harmonic frequency range is used to avoid losses of the desired signal through the DC circuit which is connected to a SMA connector.

The 300 GHz doubler chip was optimized for 10 mW of LO power per diode, i.e., the full chip is optimized for ~45 mW of LO input power between 135 – 165 GHz. The epilayer is doped at $1 \cdot 10^{17}$ cm^{-3} and it features a 350 nm thickness. The anode size of each diode is 17 μm^2, which results in a junction capacity $C_{j0} \approx 20$ fF (using eq. (2.21)). The anode size has been chosen in order to reach a nominal power of 10 mW. A value of 6 Ω for the series resistance was considered in the development of this device, using the experimental rule $C_{j0} \cdot R_S = 120\ \Omega \cdot fF$.

3.1.2 Description of the Mechanical Block

The design of the mechanical block dedicated to the 300 GHz frequency doubler used in the LO chain of the 600 GHz receiver is shown in Fig. 3.2.

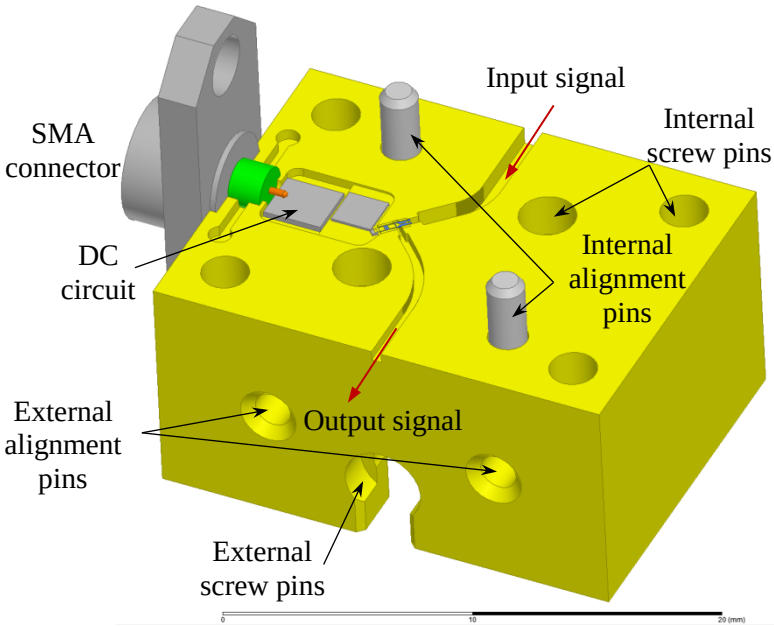

Fig. 3.2. Design of the mechanical block of the 300 GHz single chip doubler used in the 600 GHz receiver. The mounted MMIC chip and the DC circuit have been included in the image. The dimensions of the block are 15x20x20 mm^3.

The mounted MMIC chip and the DC circuit are included in fig. 3.2. The modeling was carried out with the HFSS 3D interface. The input and output signals are aligned using curved

waveguides. The external alignment pins are necessary to accurately match the waveguides with other blocks. In this case, the input waveguide needs to be aligned with the RPG 135-165 GHz doubler and the output waveguide needs to be aligned with the 600 GHz sub-harmonic mixer of the 600 GHz receiver. The internal alignment pins are necessary to correctly fit the top and the bottom part of the block. Several screws distributed throughout the full block are needed to ensure its correct closure and avoiding power leaks. The DC circuit consists of several capacities (not grounded) used to bind the SMA connector to the MMIC chip. The SMA connector is a semi-precision coaxial RF connector with a 50 Ω impedance specifically designed for signals from DC to 18 GHz.

3.1.3 Experimental Results

The experimental development and measurement of this module, whose different elements are shown in Fig. 3.3, is briefly presented in this section.

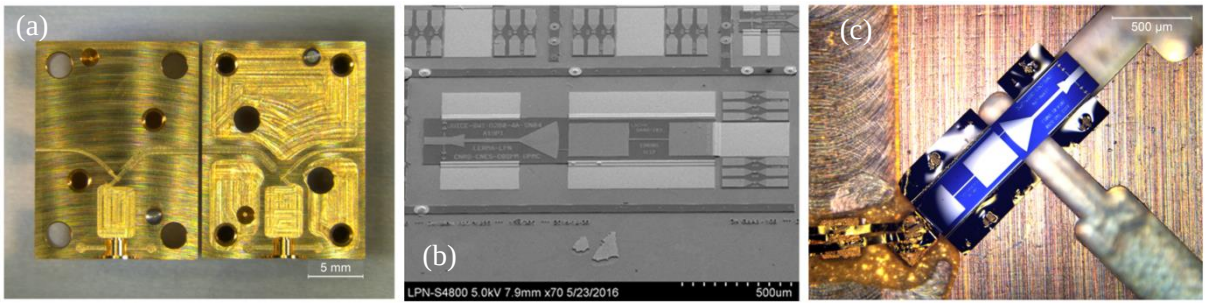

Fig. 3.3. (a) Fabricated mechanical block of the 300 GHz doubler. (b) Fabricated chips at LPN before releasing them from the wafer. (c) Mounted chip in the mechanical block at LERMA.

3.1.3.1 I-V Characteristics of the Diodes

Once the MMIC is mounted in the mechanical block it is ready to perform the measurement of the I-V characteristic of the diode cell. This measurement is the easiest way to monitor the symmetry of the PSBDs and verify a correctly balanced configuration of the circuit. The measured I-V characteristics obtained in this case are the addition of the current generated in both branches of the diode cell. Therefore the I-V characteristics presented in Fig. 3.4 are the result of dividing the raw measured voltage and current values by two, since half of the measured current flows through each branch of the diode cell and half of the applied voltage falls in each diode. The experimental DC I-V also allows the physical model of the diodes used in the ADS-HFSS simulations to be defined. The most important parameters, as discussed in the second chapter, are the ideality factor η, the built-in voltage V_B, the saturation current I_{Sat} and the DC series resistance R_S. Taken together, the I-V and the C-V characteristics of the simulated PSBDs can be defined, with the objective of approximating them as much as possible to the real diodes. The experimental results presented in Fig. 3.4 can be reasonably fitted by means of the analytical model presented in section 2.2.2 using a saturation current $I_S = 2.59 \cdot 10^{-13}$ A, an ideality factor $\eta = 1.18$, a built-in voltage $V_B = 0.765$ V and a DC series resistance $R_S = 3.6$ Ω. In order to achieve a good fit the measurements must be taken in a broad voltage range, at least reaching the built in voltage.

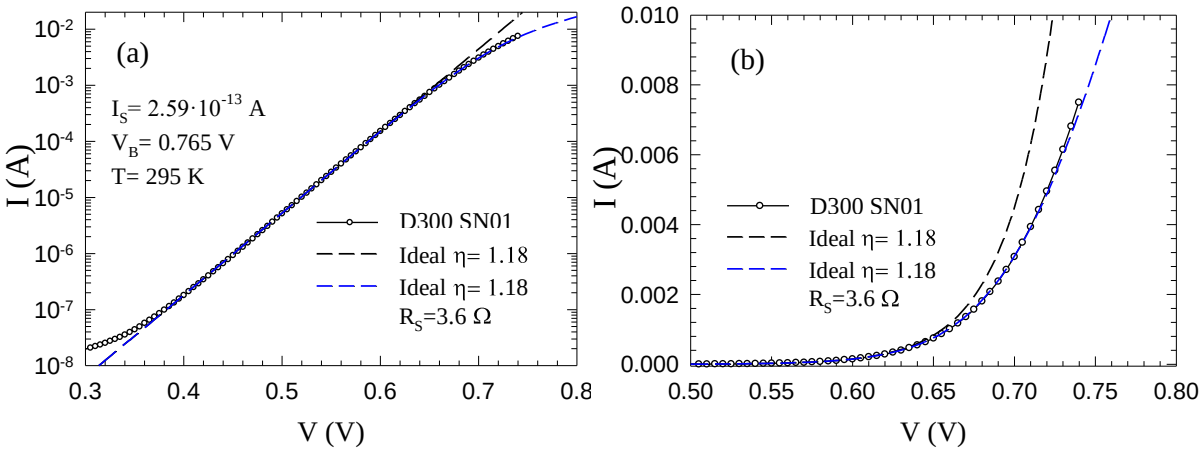

Fig. 3.4. I-V characteristics of the fabricated 300 GHz doubler MMIC mounted in the SN01 block in (a) logarithmic and (b) linear representation. The analytical fitting with and without series resistance are also plotted.

3.1.3.2 RF performance of the 300 GHz doubler

In this section we present the experimental results of the RF performance of this doubler. The scheme of the experimental test bench used for these measurements is shown in Fig. 3.5.

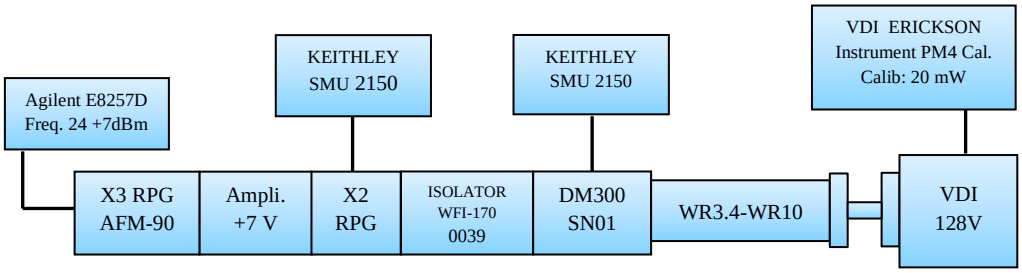

Fig. 3.5. Diagram of the experimental test bench used in the 300 GHz doubler measurement.

A 21.7 to 25.6 GHz signal from an Agilent E8257D signal generator is applied to a source which consists of a frequency tripler followed by a doubler providing output frequencies between 130 to 154 GHz. This source has been developed by Radiometer Physics GmBh (RPG). An isolator (WFI 170-0039) was then used between the output of the 150 GHz doubler and the input of the 300 GHz doubler in order to suppress the standing waves appearing between both stages. This substantially reduces the interaction between both multiplication stages and allows the accurate determination of the device performance. Unfortunately, the isolator introduces around -1 dB transmission losses and it cannot be always used in practice. The doublers are biased by Keithley SMU 2450 sourcemeters and the output measurements are obtained with a calorimeter 128 V and an Erickson PM4 from Virginia Diodes Inc (VDI). A transition from WR3.4 to WR10 was used to match the 300 GHz doubler output signal and the calorimeter inducing approximately -0.3 dB losses. The output power delivered by two different mechanical blocks, which were fabricated and mounted with the 300 GHz doubler chips, was measured using the described test bench. The results are plotted in Fig. 3.6. The power used for pumping the 300 GHz doubler is shown in Fig. 3.6 by the green line. It is in the 20-30 mW range in most of the band but it drops below when exceeding 155 GHz.The results represented in Fig. 3.6 correspond to the bias point providing the maximum output power. The experimental results of each mounted device

(black lines) have been compared with the PSBD physical models using the experimental input power and bias values.

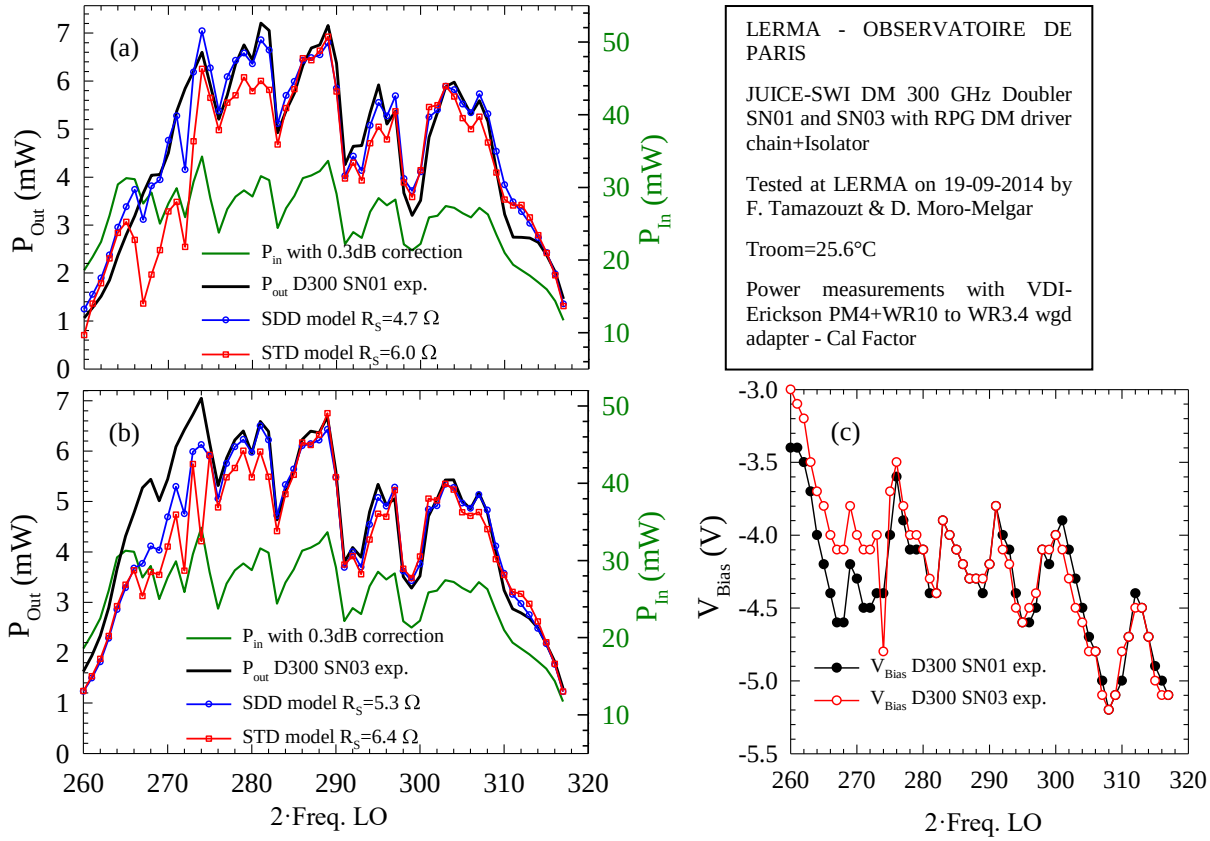

Fig. 3.6. Output power measured in two different modules (a) SN01 and (b) SN03. The experimental optimal bias is plotted in (c) for each module. The experimental results (black line) have been compared with the STD (red line) and the SDD (blue line) physical models of the PSBDs using the same parameters I_{Sat}=0.22 pA, C_{j0}= 19.4 fF and V_B= 0.79 V, while a larger series resistance has been used in the STD model (6.4 Ω) than in the SDD one (5.3 Ω).

The standard physical model (STD model) integrated in the ADS simulator and the improved capacitance model (SDD model) have been implemented using exactly the same saturation current I_{Sat}= 2.2·10^{-13} A, ideality factor η= 1.18, junction capacitance C_{j0}= 19.4 fF and built-in voltage V_B= 0.79 V (obtained from the measured I-V characteristics in DC). The only difference between both models is the dependence of the capacitance with the bias and the series resistance used to fit the experimental results (6.4 Ω for the STD and 5.3 Ω for the SDD models). In the case of the STD model, the value of R_s has to be artificially increased in order to correctly fit the output power results. The real dimensions of the mechanical block have been simulated to take into account all the losses which are not associated to the conversion efficiency of the PSBDs. Fig. 3.6 shows that both modules provide similar output power in the whole frequency band, with slightly different performances due to the variations in the resistance of the PSBDs of the MMIC, chip placement or block defects, that have strong impact mainly at the edges of the frequency band where the working conditions of the PSBDs varies due to the reduction of input power.

A good agreement is shown in Fig. 3.6, though, between the experimental results and both physical PSBD models used in ADS-HFSS simulations, where the only difference is the

analytical model of the capacitance and the simulated series resistance. In order to correctly fit the experimental output power values the series resistance to be used in the STD model has to be ~1.25 times larger than that of the SDD model. It is demonstrated in this section that the same simulated I-V characteristic leads to higher conversion efficiency within the STD model due to the lower average capacitance in one period signal. Regarding the agreement between experimental results and simulations, the output power is accurately predicted by both analytical models above 283 GHz of output frequency signal (even when simulating different series resistances). The improved SDD model seems to be more accurate than the STD model at frequencies below 283 GHz, even if the dispersion of the experimental results does not allow a perfect comparison. None of these models is able to fit the high output power values of the module SN02 at low frequencies, Fig. 3.6(b), which are probably associated to a geometrical difference between the experimental mechanical block and the simulated one.

Although Fig. 3.6 shows that the SDD model seems to provide a better agreement with the experimental results than the STD model, this comparison is not sufficient to validate the advantages introduced by the improved capacitance model since the experimental results can be satisfactorily fitted by both models. In order to reach a conclusion further analysis is required, since only the raw measured output power has been considered in Fig. 3.6, without taking into account that a bias optimization has been carried out at a single input power in the 20-30 mW range.

3.1.4 Experimental Comparison Between PSBD Physical Models

This section is dedicated to a deeper analysis of experimental results of the 300 GHz doubler and the physical PSBDs models available. Another MMIC was mounted in the SN01 mechanical block and was first measured at different constant input powers where the bias was optimized for each frequency in order to reach the maximum output power. The delivered output power was then measured when sweeping the bias at fixed input power and frequency. In order to perform such measurements a bidirectional coupler and a tunable attenuator were included in the experimental test-bench, shown in Fig. 3.7, for adjusting the power injected into the 300 GHz doubler. The directional coupler allows measuring the power reflected by the isolator with the 154V calorimeter (which is in the range of -14 to -10 dB), so that we can accurately determine the input power arriving to the 300 GHz doubler (after performing the calibration of the system by connecting the 128V calorimeter directly to the isolator), and adjust it by means of the attenuator. In addition, -0.3dB of transmission losses in the WR3.4-WR10 section and the calorimeter have been considered. This conceptual approach to fix the input power in the desired device has also been used in [Siles15]. The experimental test-bench proposed in Fig. 3.7 has allowed us to measure, on one hand, the output power delivered by the 300 GHz at 15, 20, 25 and 30 mW of constant input power and on the other hand, the dependence of the output power when sweeping the chip bias for fixed input power and frequency values.

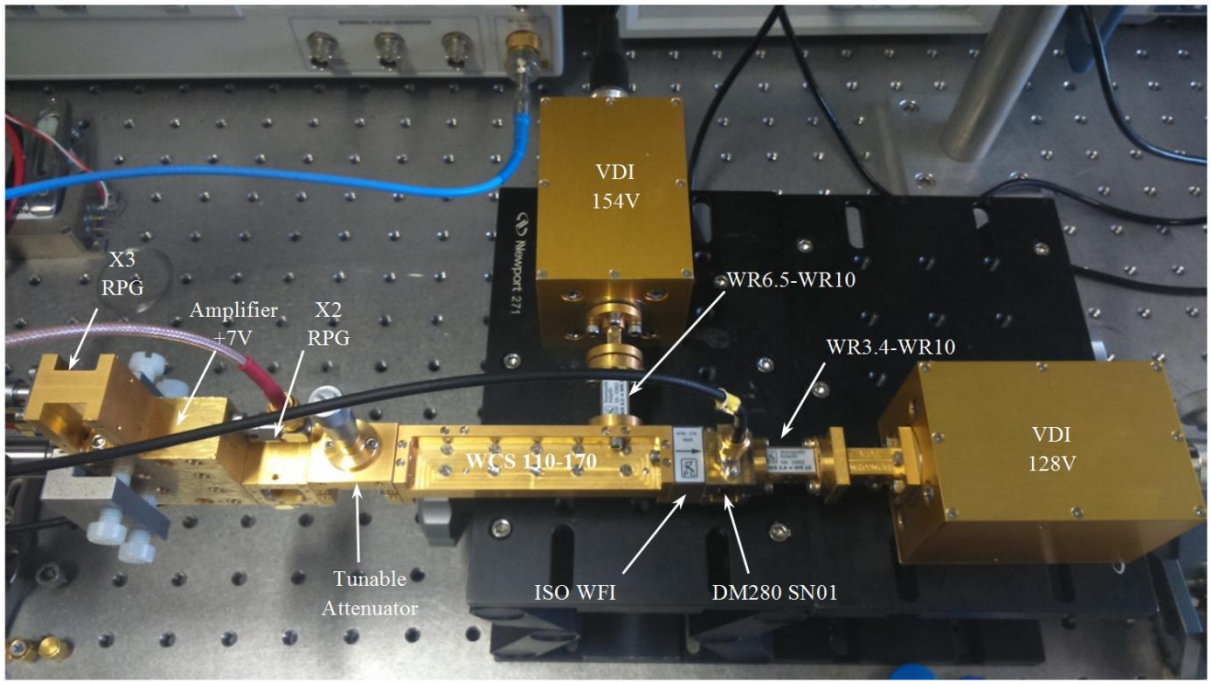

Fig. 3.7. Experimental test-bench used in the analysis of the 300 GHz doubler at fixed input power.

3.1.4.1 Performance at Constant Input Power

The analysis of the 300 GHz doubler SN01 carried out using the experimental test bench shown in Fig. 3.7 has enabled the measurement of output power when fixing the input power at 15, 20, 25 and 30 mW of input power, Fig. 3.8. The DC current value generated in the chip in RF conditions was also measured in this analysis and plotted in the Figure.

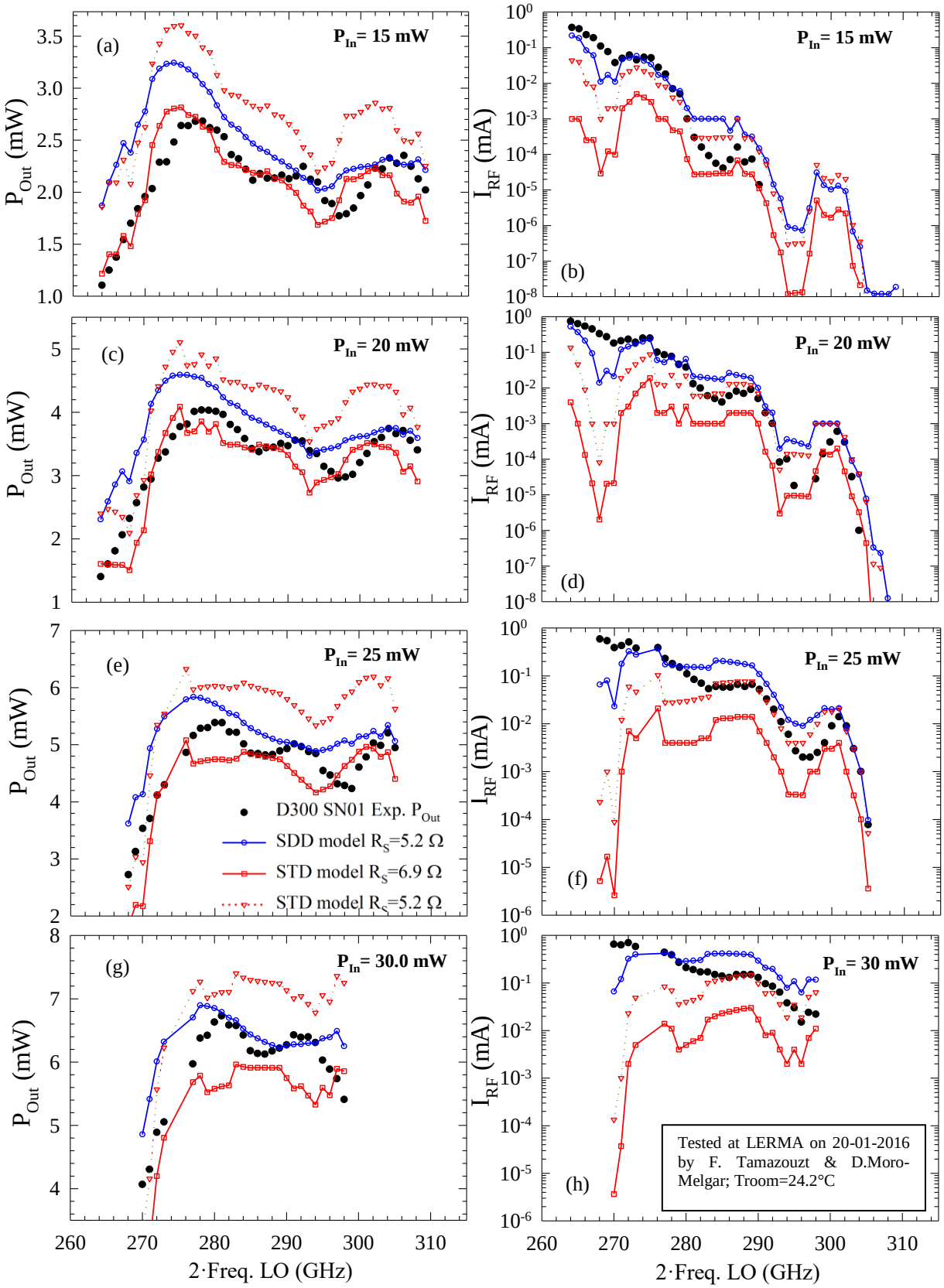

Fig. 3.8. Measured values (black dots) of the output power (a), (c), (e), (g) and the DC current in RF conditions (b), (d), (f), (h) when optimally biasing the 300 GHz doubler chip with a fixed input LO power at 15, 20, 25 and 30 mW respectively. The simulated input power has been corrected in a 0.3 dB factor. The legend shown in Fig (e) and the represented frequency band affects all the figures. The results of the STD model are represented by the red dotted lines and the SDD model predictions are represented by blue doted

lines. Two values of the series resistances have been used in the case of the STD model, 5.2 Ω (the same used in the STD model, plotted with red circles) and 6.9 Ω (the value providing the best agreement with the experimental results, plotted with red squares).

The optimal bias has been optimized for each point to obtain the highest output power, and the corresponding bias current value was measured in the 300 GHz chip. The conversion efficiency depends on the frequency and the input power, and it varies from ~16 % at 15 mW to 22 % at 30 mW according to Fig. 3.8. The experimental results have been compared with the analytical STD and SDD models in our ADS-HFSS test-bench. The same saturation current I_{Sat}= 2.59·10^{-13} A, ideality factor η= 1.18, junction capacitance C_{j0}= 19.7 fF and built-in voltage V_B= 0.765 V are defined in both models. The value of the series resistance for each model has been adjusted to fit the experimental results as much as possible, where the high frequencies of the band (around 300 GHz) have been considered as reference since, as shown in Fig. 3.6, they show lower dispersion. The simulated series resistance is 1.3 times higher in the STD model (R_S=6.9 Ω) than in SDD ones (R_S=5.2 Ω), similar to the difference found in Fig. 3.6. An additional comparison between STD and SDD models is included in Fig. 3.8 when using the same simulated I-V characteristic, i.e., considering the same value of the series resistance (5.2 Ω). The experimental output power is reproduced to a greater degree by the STD model with R_S=6.9 Ω , however, the SDD model presents a superior agreement with the measured current.

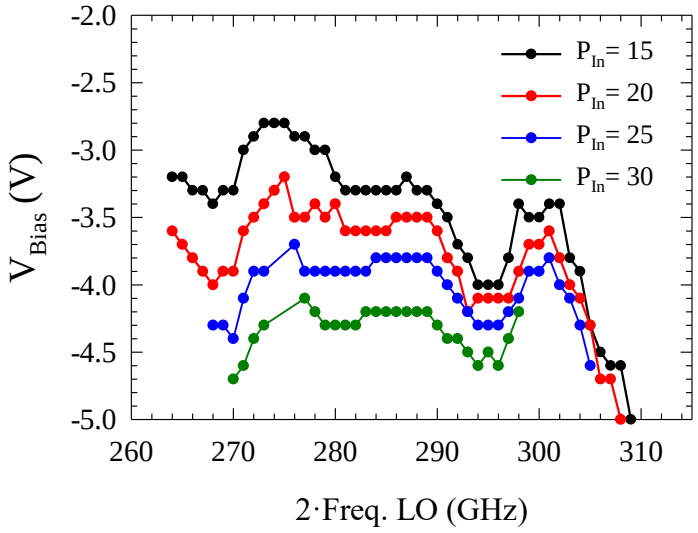

Fig. 3.9. Experimental optimal bias used to obtain the best output power in the 300 GHz when fixing the input power at 15, 20, 25 and 30 mW.

The current results presented in Fig. 3.8 have a typical tendency found in all our frequency doublers at this frequency range, which is predicted by our simulations. The current at high frequencies of the band is very low and it increases for the lower frequencies (even up to some milliamperes). The reason is that the higher the frequency is, the smaller the amplitude of the voltage signal excited in the PSBDs when fixing the input power. This factor is exploited during the optimization process of the MMIC chip to take advantage of the second harmonic generation in the low/high voltage range of the C-V characteristic in the high/low frequency sides of the band and can be easily understood when analyzing the dependence of the experimental optimal bias with the frequency, plotted in Fig. 3.9. It shows that the optimal bias decreases at the upper side of the frequency band, especially at low input power values.

This, together with the fact that the amplitude of the voltage signal generated in the PSBDs is lower for the higher frequencies, makes the diodes work in a pure varactor mode in that frequency range, while it changes to a varactor-varistor mode in the lower frequency side (lower bias voltage but larger amplitude of the sweep). The higher series resistance needed by the STD model to fit the experimental output power results explains why it underestimates the current, especially in the low frequency side, where the voltage signal in the PSBDs is closer to flat band conditions.

We finish this section comparing the PSBD physical models when considering the same series resistance R_S= 5.2 Ω in both models. We can now recognize an improvement of the agreement with the measurements of the current predicted by the STD model with this lower series resistance. Now the results of both STD and SDD models practically coincide in the upper side of the frequency band (corresponding to low currents), but STD still predicts excessively low values of current as the frequency decreases. Regarding the output power, the STD model overestimates the conversion efficiency even more than the SDD model when simulating the same I-V characteristic. The fact that the STD and SDD models are almost equivalent at very low current values and the better predictions given by the SDD model when the current increases indicates that the improved impedance model enhances the prediction capabilities of the simulations. Additionally, within the SDD model the simulated series resistance corresponds to that extracted from the DC measurements of the diodes (Fig. 3.4) so that the accuracy of the predicted performance of a hypothetical module using different diodes can be improved.

3.1.4.2 Optimal Bias Analysis

The experimental results of the output power and the current when optimizing the chip bias have been compared in detail in the previous section with both analytical models. However, we still need to compare the experimental optimal bias and the predicted optimal bias by each analytical model in order to conclude the contribution of the improved model in the design of frequency doublers. The measurement of the output power and current when sweeping the chip bias for a fixed input power and frequency is now necessary. The measurements have been performed at output frequencies 270, 277, 287, 297 and 304 GHz, whenever possible, when fixing the input power at 15, 25 and 30 mW.

The case at 15 mW of input power is analyzed in Fig. 3.10 where the experimental output power (black dots) when sweeping the chip bias from -1 V to -5.8 V, has been plotted and compared with the STD and the SDD model. Results presented in Fig 3.10 contain the experimental values (black dots) compared with the improved capacitance model SDD (blue dotted line) with R_S= 5.2 Ω and the standard STD model (red dotted line) with R_S= 6.9 Ω. The additional case where the same series resistance R_S= 5.2 Ω has also been used in the STD model, allows the role of the series resistance in the optimal bias prediction to be compared. The experimental optimal bias presented in Fig. 3.9 are indicated in each case in Fig. 3.10 by the vertical black lines which indicate the bias point where the 300 GHz doubler provides the highest output power. It is remarkable that in Fig. 3.10.(a) and (d) that none of the analytical models correctly predict the experimental results obtained at 270 and 297 GHz. However, the SDD model at 277, 287 and 304 GHz reproduces satisfactorily the measured optimal bias

values and output power dependencies, in spite of overestimating the maximum output power at 277 GHz.

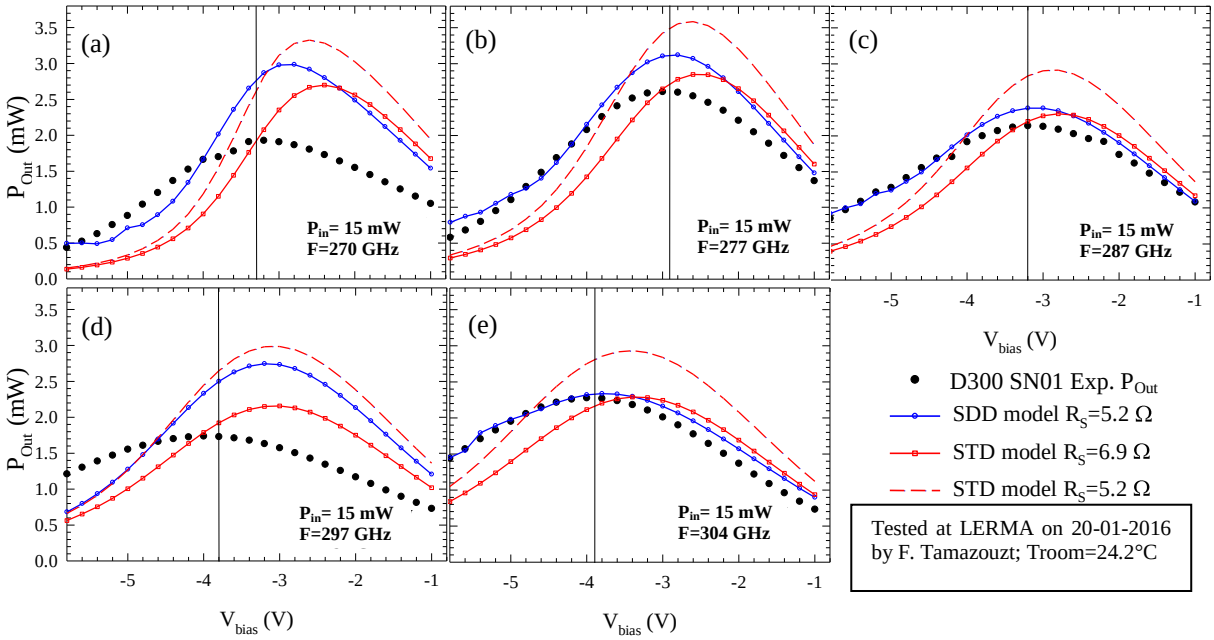

Fig. 3.10. Experimental output power (black dots) of the 300 GHz doubler SN01 when sweeping the chip bias from -1 V to -5.8 V at 15 mW of input power and output frequencies 270, 277, 287,297 and 304 GHz. The same legend and axes are used by all figures. The optimal bias is indicated by the vertical solid black line.

Regarding the STD model, it predicts a reverse optimal bias lower than the experimental one in all cases for both simulated series resistances. The discrepancy is the highest, even reaching 0.5 V, when using R_S= 6.9 Ω. However, as shown before, this artificially high value of R_S is necessary in order to reproduce the experimental output power along the band at the experimental bias, which does not correspond with the optimal bias predicted by this model. It means that the considered R_S= 6.9 Ω value for the STD model, when analyzing the results presented in Fig. 3.8, is misrepresenting the comparison with the experimental results. The SDD improved model does not exactly predict the measured values of output power but the optimal bias is modeled adequately since the series resistance considered has a real correspondence with the experimental values.

We can extract the same conclusions from Figs. 3.11 and 3.12, where the output power vs. applied bias for different frequencies obtained at 25 and 30 mW input power, respectively, have been plotted. In Fig. 3.12 only the results for 270 and 297 GHz are shown because the output power at 277, 287 and 304 GHz was not enough to obtain any measurement. In both cases at 270 GHz and 297 GHz both STD and SDD models fail again [even if the disagreement is reduced for 30 mW of input power, Fig. 3.12(b)], but the SDD model works very well at 277, 287 and 304 GHz. In summary we can see that the SDD model is able to correctly predict the optimal bias in most of the band using the series resistance estimated from the I-V curves of the diodes. On the contrary, the STD model predicts a lower optimal reverse bias than the SDD model in all cases even if the same I-V characteristic (same R_S= 5.2 Ω) is simulated. Moreover, in order to better reproduce the optimum bias point with the STD model, the value of the series resistance used should be artificially lowered. This would lead

to a stronger disagreement on the expected output power since, as we saw in Fig. 3.8, the value of R_S must be increased in order to obtain a good agreement with the experimental results.

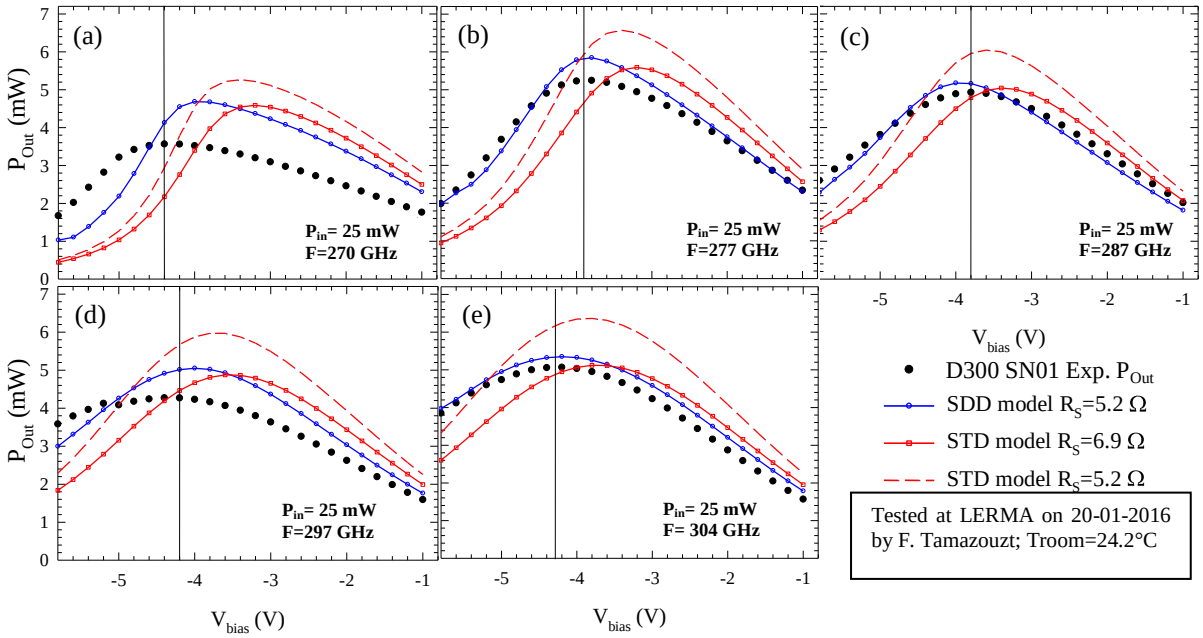

Fig. 3.11. Experimental output power (black dots) of the 300 GHz doubler SN01 when sweeping the chip bias from -1 V to -5.8 V at 25 mW of input power and output frequencies 270, 277, 287,297 and 304 GHz. The same legend and axes are used by all figures. The optimal bias is indicated by the vertical solid black line.

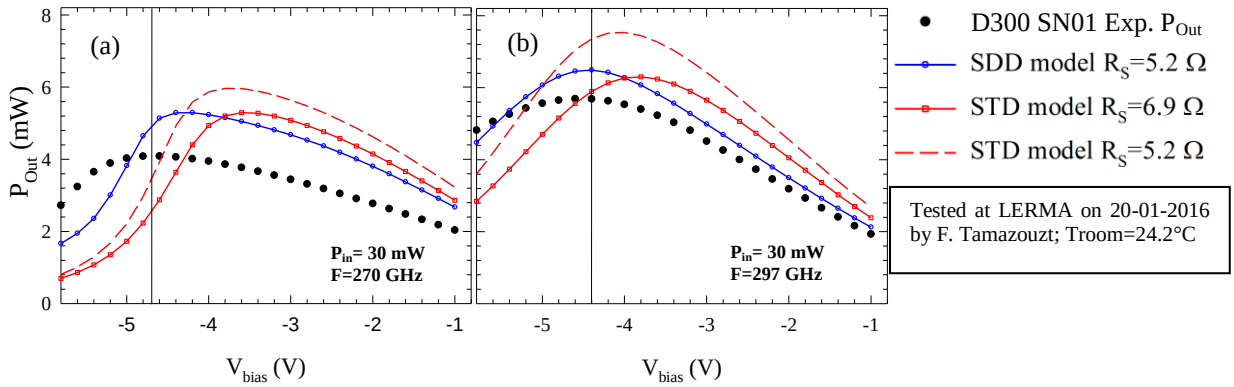

Fig. 3.12. Experimental output power (black dots) of the 300 GHz doubler SN01 when sweeping the chip bias from -1 V to -5.8 V at 30 mW of input power and output frequencies 270 and 297 GHz. The same legend and axes are used by all figures. The optimal bias is indicated by the vertical solid black line.

These observations can be condensed since the capacitance model implemented for the PSBD in the SDD analytical model uses consistently the I-V and the C-V data, and is able to keep the physical meaning of the series resistance of the diode. This conclusion lays the basis for developing an improved resistance model (in which current saturation and carrier inertia, for example, were considered) able to correctly predict the performances of other types of modules (mixers, detectors, etc.) working at different frequencies where the physical properties of the PSBDs need to be changed.

3.2 A Power-Combined 300 GHz Frequency Doubler

The single chip 300 GHz doubler presented in section 4.1 is able to efficiently handle around 40-60 mW input power, while the source developed by RPG for the 1.2 THz channel of the JUICE-SWI instrument can achieve more than 60mW across the full 135-160GHz band. Therefore, an improved 300 GHz doubler is required to be able to manage this power. A new mechanical block, able to feature two 300 GHz chips, is presented in this section. This results in a 300 GHz power-combined doubler that is able to handle up to 120mW. First, it is necessary to define an input structure able to split the input power in order to equally pump two different MMIC chips and another structure at the output to join the generated output signals back together. The typical structure we can find for this purpose is the so-called "Y-junction", which splits the input signal while keeping in phase both input and output signals, e.g., the power-combined tripler in [Siles15]. However, this configuration is not suitable for the input stage of our module due to the longitudinal orientation of the MMICs with respect to the input waveguide that involves a symmetrical placement of the two MMICs at the output of the module. This design requires the use of a quadrature hybrid coupler that produces a 90º phase shift between the input signals pumping each of the doublers in order to ensure the correct alignment of the field lines at their output, as we will see in this section.

3.2.1 Quadrature Hybrid Coupler

The structure proposed by LERMA for splitting the input power that pumps each doubler chip is presented in Fig. 3.13. It is a so-called "quadrature hybrid coupler," that allows dividing the incoming power while introducing a 90º phase shift between the signals at the output ports of the structure. This kind of passive waveguide element has already been used in the 400-500 GHz SIS mixer of [Seri08].

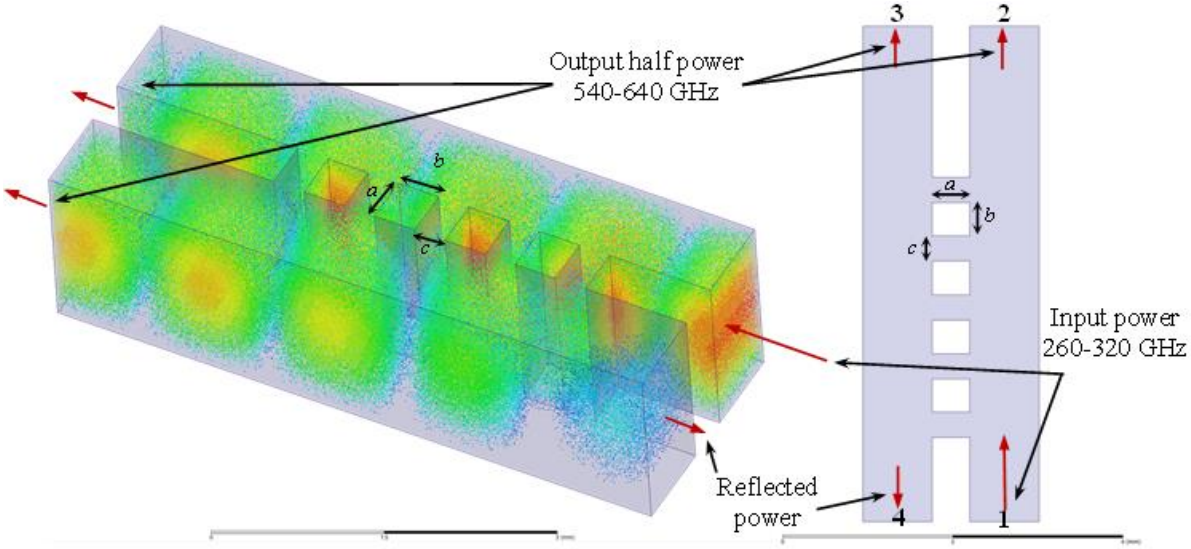

Fig. 3.13. Quadrature hybrid coupler as simulated in the HFSS software. The distribution of the electric field magnitude for an input signal of 150 GHz is shown at a given time instant in order to appreciate the 90º phase shift at the output stage. Red lines represent the main direction of the signal and the main dimensions of the coupling cavities are represented by *a*, *b* and *c*.

The hybrid structure, designed Dr. A. Maestrini using the HFSS software, is presented in Fig. 3.13, where the 3D distribution of the electric field magnitude for an input signal of 150

GHz is also shown at a given instant. The input signal arrives into port 1 and progressively leaks into the second waveguide, coupled by the cavities. The dimensions and the number of coupling sections represented in Fig. 3.13 by *a*, *b* and *c* need to be optimized to minimize the transmission losses (less than -3 dB are required) from the input to each of the output ports 2 and 3, while correctly introducing a 90º phase shift between them in the considered frequency band.

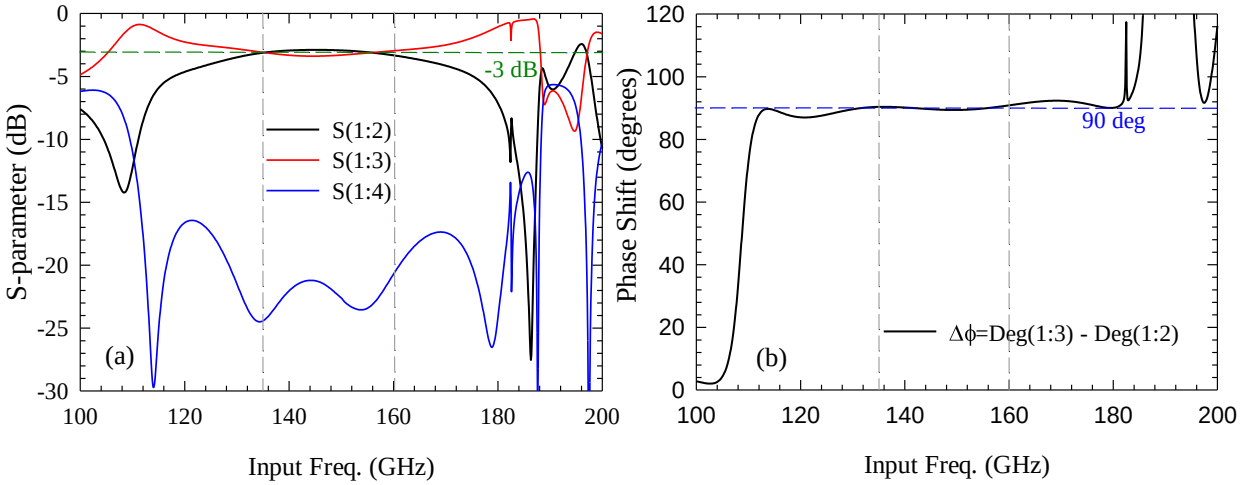

Fig. 3.14. Results of the simulation of the quadrature hybrid coupler using the HFSS software: (a) transmission losses of ports 2, 3 and 4 and (b) phase shift between the output ports 2 and 3. The vertical grey dashed lines indicate the desired frequency band where the structure is expected to operate. The requirements of –3 dB losses and 90 degree phase shift are also indicated in each figure.

The company in charge of the fabrication of the mechanical blocks, SAP-Micro, is able to manufacture coupling sections with a minimum width of 300 µm for a rectangular waveguide of 826 µm x 1652 µm. Taking into account that constraint, the final optimization consists of 5 coupling sections where a = 450 µm, b = 400 µm and c = 300 µm. Once the structure is optimized, a negligible amount of power (losses higher than -20 dB) should leak to port 4. Since the output signals of this structure will be connected to the 300 GHz chips, which behave as mismatched loads, there will be a reflected signal that will come back out of the structure through ports 1 and 4. As a result, a matched impedance load is usually connected to port 4 in order to absorb as much as possible the reflected signal. The simulations of the quadrature hybrid coupler presented in Fig. 3.13 have been provided with the HFSS software considering a conductivity of the metal waveguide surface of $2 \cdot 10^7$ S/m. The results are plotted in Fig. 3.14 where the desired frequency band is delimited by the vertical dashed lines. The transmission losses from the input port to the rest of the ports are plotted in Fig. 3.14(a), showing that the losses to ports 2 and 3 are lower than -3 dB while those to port 4 are higher than -20 dB in the full optimized band. The 90 degree phase shift between the output signals in the ports 2 and 3, shown in Fig. 3.14(b), is also confirmed in the full 135-160 GHz band.

3.2.2 Description of the Matching Network Design

Once the input signal is correctly divided and phase shifted, it is necessary to optimize the matching network to allow the 300 GHz doubler chips to correctly manage the input power. The dimensions of the output Y-junction have been reduced as much as possible because the closer the chips are, the closer the 90 degree hybrid junction can be placed to them, thus obtaining a very compact mechanical block. The final geometry of the output Y-junction and the electric field vector in the waveguide system are presented in Fig. 3.15, where the combined chips have been simulated in HFSS at 320 GHz. The electric field vector has been simulated by including a 180 degrees phase shift between the 320 GHz signals generated by each chip, which results from doubling the phase shift between the input signals. Moreover, the distance between chips has been reduced to 1276 µm which is exactly the width of the hybrid coupler presented in Fig. 3.13. The chips have been perfectly aligned with the input waveguide, thus obtaining the most compact configuration possible. Regarding the electric field vector, the output of both chips are in opposite phase, but the symmetrical configuration of the antennas with respect the output waveguides allows both signals to be back in phase when they reach the Y-junction intersection.

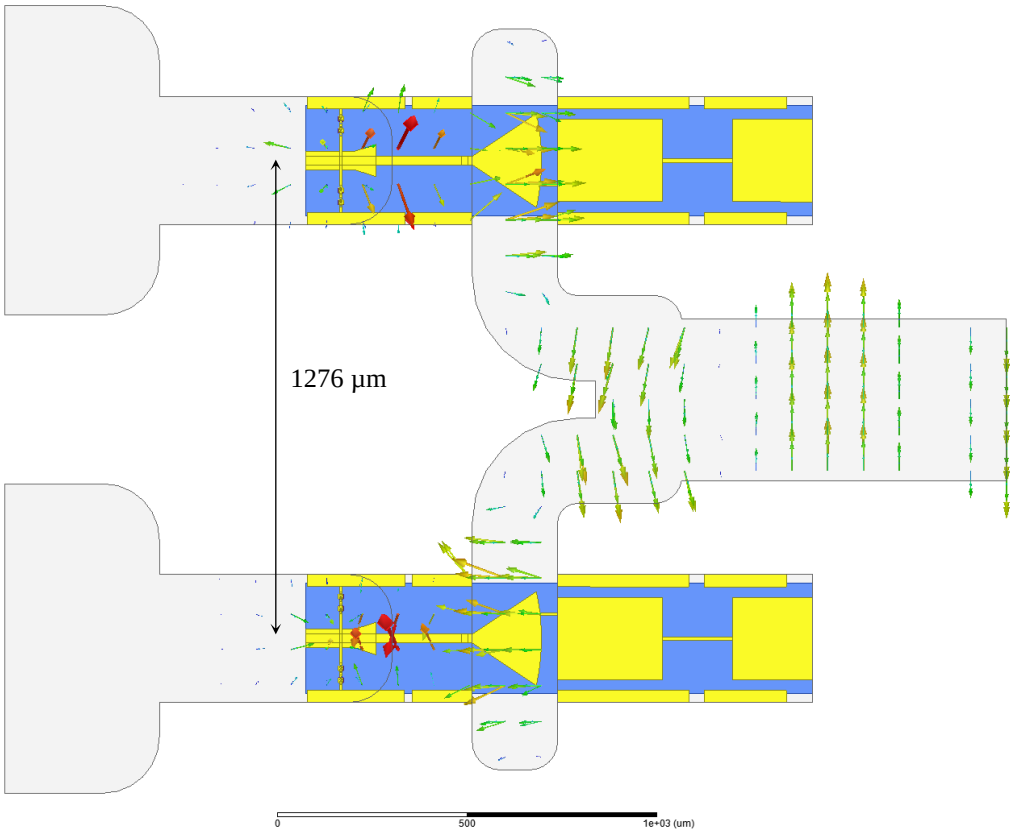

Fig. 3.15. Configuration of the output Y-junction used to combine the output signals generated by the two doubler chips. The electric field vector has been simulated by HFSS at 320 GHz considering a 90º phase difference between the input signals.

3.2.3 Mechanical Block Design: DC Circuit

The design of the mechanical block can now be defined according to the dimensions of the hybrid coupler and the output Y-junction. Additional complexity in the design has been

introduced since it is now required to have DC circuits to bias both chips. A design with just one input bias connector was finally proposed by LERMA, thus avoiding one additional connector in the mechanical block, but the drawback is that it requires defining an additional DC path which has to pass below the waveguide system. The final design of the 300 GHz power-combined block in HFSS is represented in Fig. 3.16, where the different elements of the RF and DC circuits are indicated. The thickness of this highly compact block is only 10 mm, lower than the single chip module presented in Fig. 3.2. Indeed, the screws and the internal alignment pins have been the limit factor to reduce the thickness of the block. The doubler chips are aligned with the 90º hybrid coupler whose fourth port is finished in a matched load that absorbs at least half of the reflected signal, thus intrinsically improving the return losses of the module as compared with the single chip block.

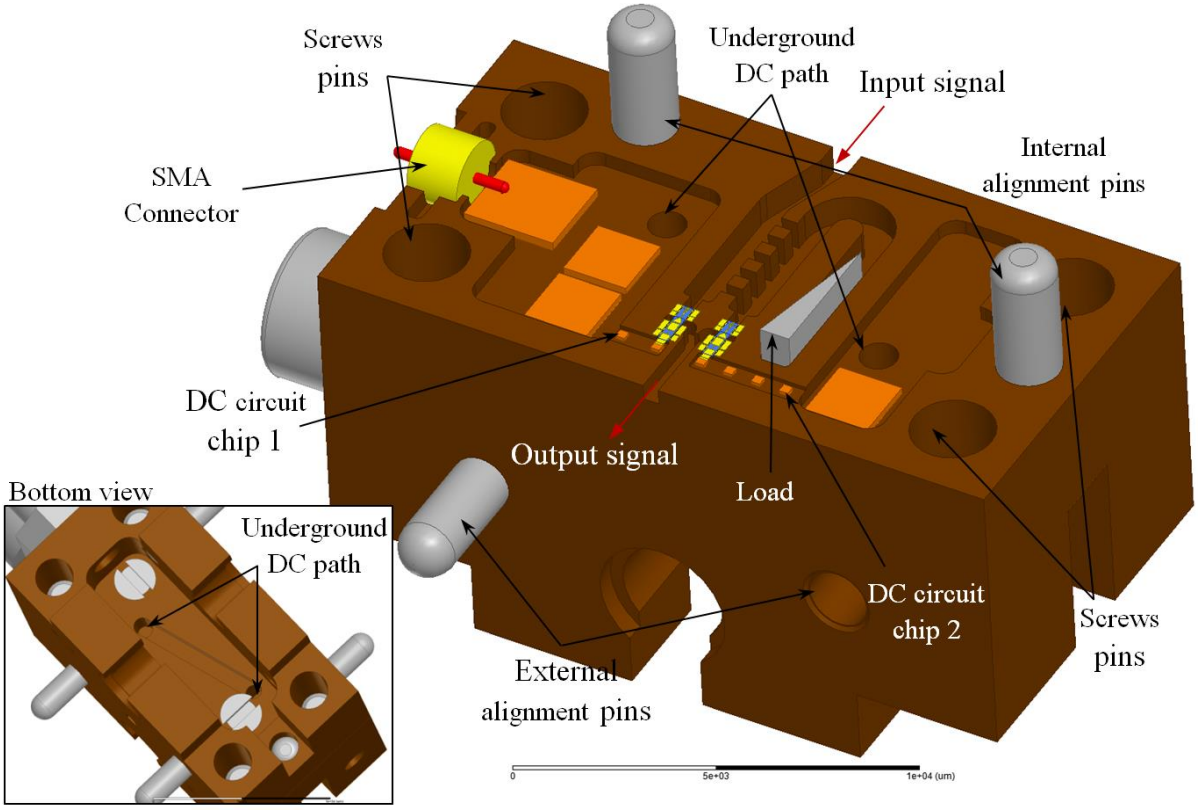

Fig. 3.16. 300 GHz power-combined block with the different elements indicated. A bottom side view of the block is shown in the small image to illustrate the implementation of the additional DC path. The dimensions of the block are 10x19x20 mm^3.

The additional DC path to bias the chip, placed in the opposite side of the SMA connector, has been implemented with two vertical holes that go through the block at each side of the waveguide. An isolated cable is used in the mounting process to pass through this additional path and to connect the second chip. An isolated cable is used in the mounting process to pass through this additional path and to connect the second chip. The DC circuit uses several capacitors bonded each to other and attached to the block with non-conductive glue in order to isolate the DC path from the mechanical block.

3.2.4 Experimental RF Performance

The fabricated block, whose different elements are shown in Fig. 3.17, provide I-V characteristics similar to those shown in Fig. 3.4 for the single-chip block. In this case both chips are biased by the same source and the I-V curve measured corresponds to the contribution of the eight PSBDs. Therefore, it is not possible to exactly determine if there are deviations in the I-V characteristics of the different diodes but the results presented in Fig. 3.4 can be considered as a good reference since they belong to the same fabrication run.

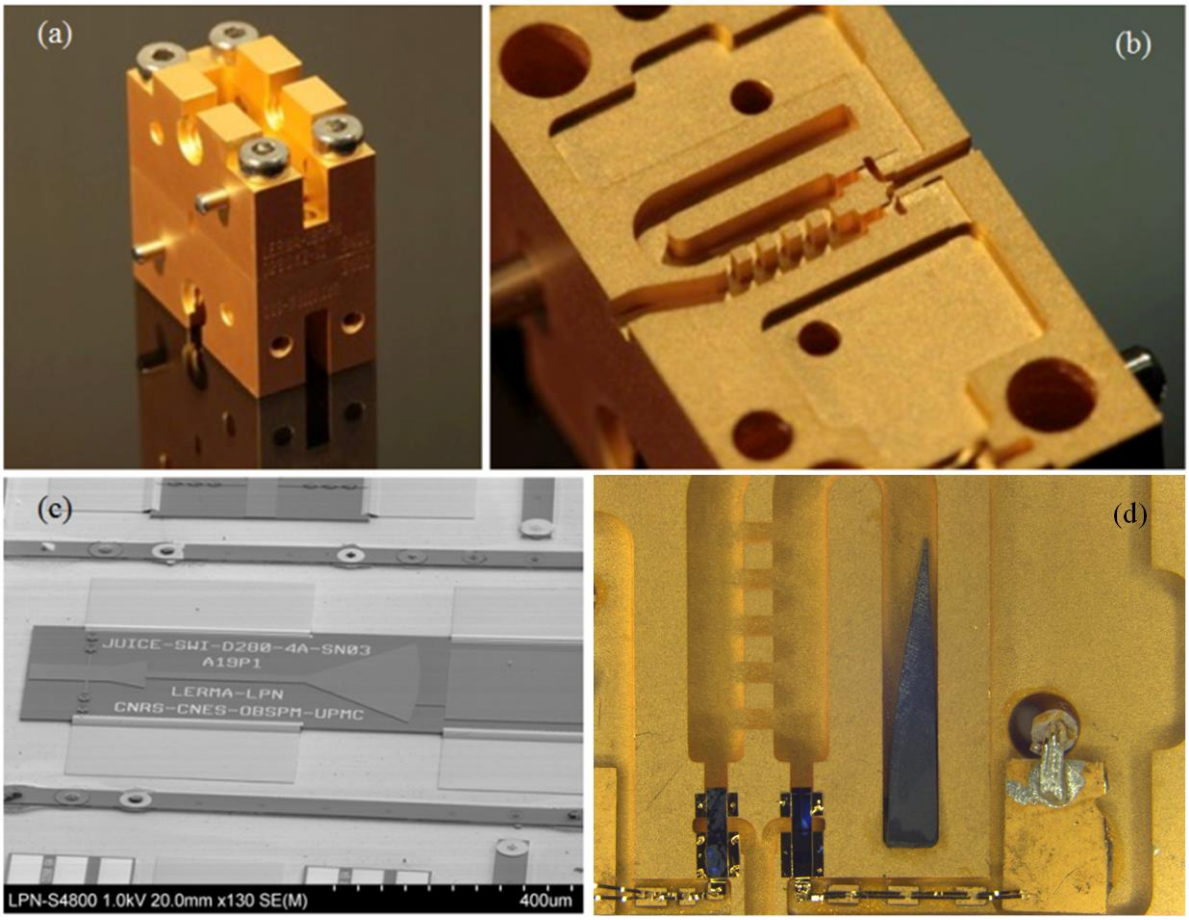

Fig. 3.17. (a) and (b) Photographs of 300GHz power-combined doubler block fabricated by SAP-micro before assembly. (c) Photograph of the MMIC 300 GHz doubler chip fabricated by LPN before being released from the wafer. (d) The two MMIC chips at 300 GHz and the load mounted in the mechanical block.

The montage used to characterize the 300 GHz power combine doubler is presented in Fig. 3.18. The RPG DM driver chain at 150 GHz has been pumped with an Agilent E8257D signal generator between 21.7 GHz to 25.6 GHz that is multiplied by a frequency tripler before amplifying the resulting signal with two amplification stages. The signal between 65.1 GHz to 76.8 GHz is power split to pump two different frequency doublers able to deliver more than 60 mW of LO power between 135 – 160 GHz. The transition between the 150 GHz RPG source and the 300 GHz power combined doubler consist of a 0.691 mm polarization rotator shim, able to turn 90º the electric field vector of the TE_{10} mode, and a 20 mm WR-6 waveguide section. The output power of the RPG source was measured using a WR3.4 to

WR10 waveguide section to match the VDI PM5 calorimeter waveguide section. The bias for the different elements is provided by Keithely SMU 2450 units.

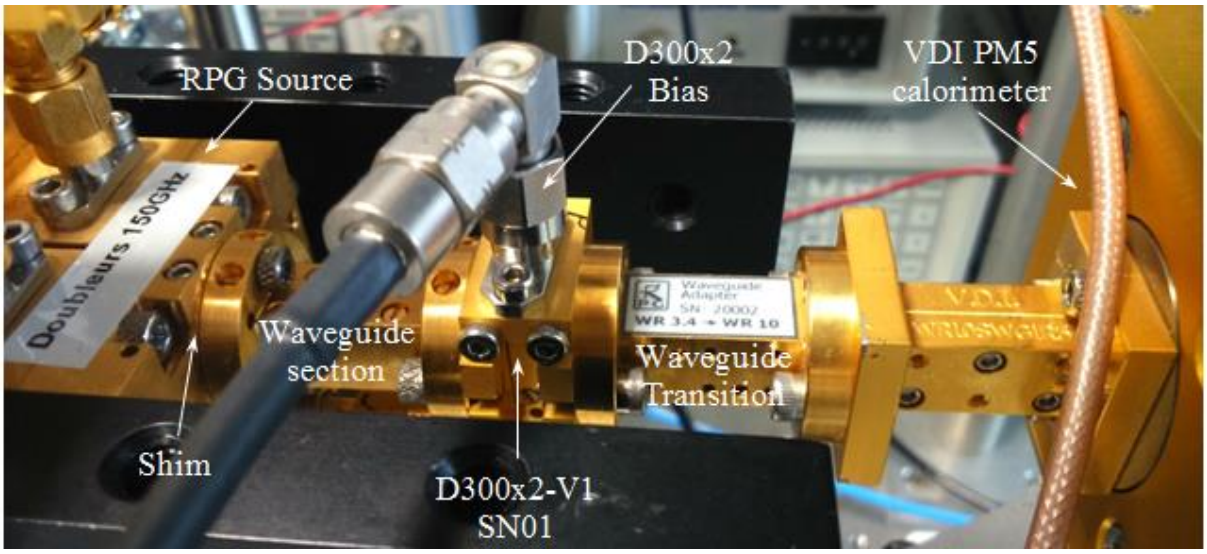

Fig. 3.18. Test bench used to characterize the 300 GHz power combined doubler using the RPG DM driver chain developed for the 1.2 THz channel. The different elements have been indicated.

The measurements have been automatized using the Labview software, thus the results presented in this section have been obtained in the same way under the same laboratory conditions. The output power delivered by the 300 GHz power-combined doubler has been plotted in Fig. 3.19, where the bias has been optimized aiming for the best output power performances. It also includes a plot of the measured power of the pumping signal provided by the RPG DM driver chain, and the corresponding efficiency. Conversion efficiencies between 23-25 % are provided by the power combined doubler, even exceeding expectations since the design was made aiming to a 60 mW input power and 20 % of efficiency in the 270-320 GHz band.

Tested at LERMA on 11-08-2016 by A. Maestrini, A. Feret and D. Moro-Melgar; Troom=21-22°C

Power measurements with VDI-Erickson PM5+WR10 to WE3.4 wgd adapter;

Cal Factor= 0 dB

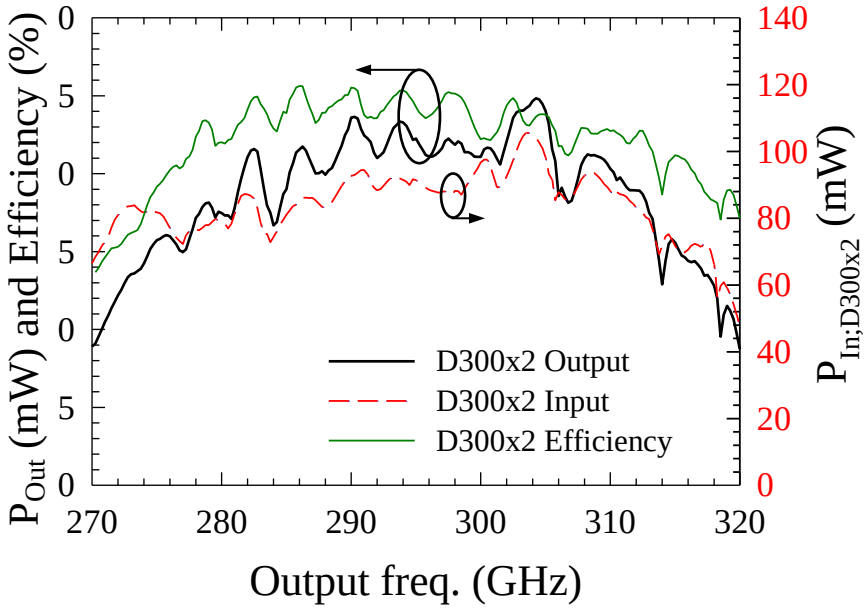

Fig. 3.19. Output power (black line) delivered by the 300 GHz power combine doubler when pumping it with the RPG DM driver chain delivered power (dashed red line). The conversion efficiency is estimated (green line).

No hint of standing waves generated by the reflections between the RPG source and the connected 300 GHz doubler is observed in Fig. 3.19, as expected. This is due to the low return losses of this doubler (due to the quadrature hybrid coupler) and the long transmission path of the reflected signal introduced by the 20 mm waveguide section. The efficiency is better than that of the single chip doubler which is around 20 % (Figs. 3.6 and 3.8). This improvement is associated with the decrease of the return losses provided by the quadrature hybrid coupler and an input power level closer to the optimum one for the design of the MMIC chips (~ 45 mW input power). The output power delivered is above 15 mW in most of the frequency band and reaches 22-23 mW in the center. However, the output power drops fast at the edges of the frequency band, where only ~10 mW are obtained. The low conversion efficiencies in the lower frequency range can be explained by the problems in the mounting of the MMIC chips in the mechanical block (as already observed for the single-chip block).

This 300 GHz power-combined doubler will be used to pump the 600 GHz doubler that will be presented in chapter 5, but we will first analyse in next section the ADS-HFSS simulations of this block.

3.2.5 Comparison with ADS-HFSS Individual Simulations

A precise test bench has been defined in ADS-HFSS simulations where the dimensions of the designed mechanical block of Fig. 3.16 have been accounted for. A batch simulator has been used in ADS to define the set of experimental values used at each frequency in both the input power delivered by the RPG source and the optimal bias of the 300 GHz power-combined doubler to maximize the output LO power between 270 GHz and 320 GHz. Transmission losses of 0.1 dB are considered in the measurement of the delivered power by the RPG source and 0.3 dB are considered in the measurement of the output power delivered by the 300 GHz power combine doubler due to the calorimeter system. The parameters for the simulation of the PSBDs are exactly the same used in section 4.1.4.1 for the SDD model (the MMIC chips are exactly the same and were fabricated in the same run of those used for the single chip 300 GHz doubler): saturation current I_{Sat}= $2.59 \cdot 10^{-13}$ A, ideality factor η= 1.18, junction capacitance C_{j0}= 19.7 fF, built-in voltage V_B= 0.765 V, T= 295 K and series resistance R_S= 5.2 Ω (the same used in Fig. 3.8).

An additional study has been included in this section. The consideration of the small signal equivalent RLC circuit associated to the dynamic epilayer impedance, presented in Chapter 2 section 2.2.3, has been taken into account in this section to compare the prediction capabilities introduced by this model in the LEC model of the PSBDs. This study allows us to understand how the addition of the RLC equivalent circuit affects the results predicted by the harmonic balance ADS simulator and it will allow us to assess the usefulness of this model for the PSBDs optimization. The value of R_E in the epilayer RLC circuit has been calculated using our 2D-MC simulator in DC conditions, that provided a value of around 2 Ω, which is in good agreement with the value proposed in [Louh95]. The comparison between the experiments and the ADS-HFSS simulation results are plotted in Fig. 3.20 The ADS-HFSS simulations were performed using the developed SDD model with the experimental values of the input power and bias when i) considering the constant series resistance model and ii) an RLC circuit modeling of the epilayer.

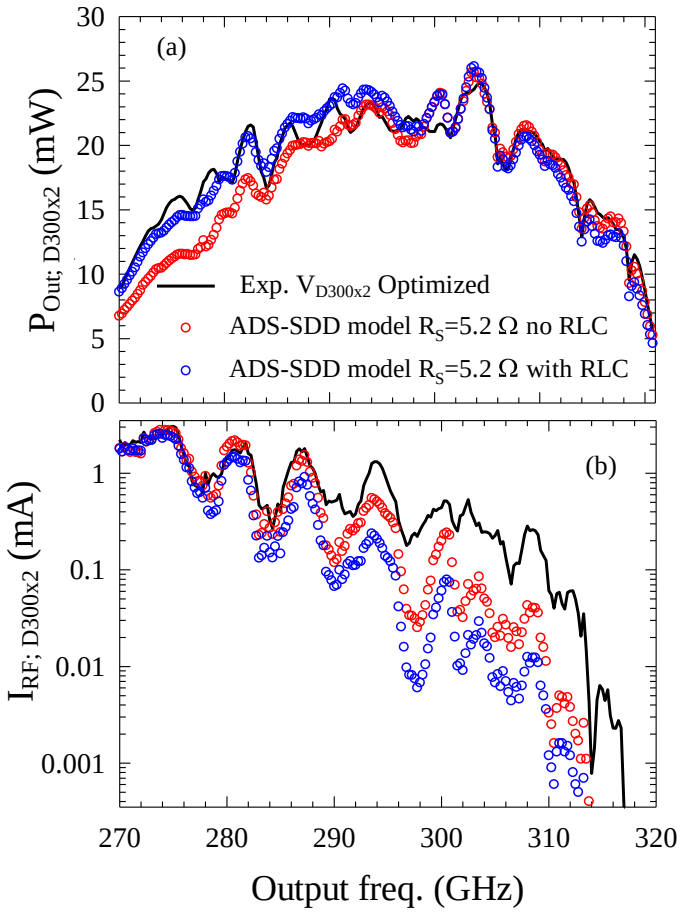

Fig. 3.20. Comparison between the experimental (black line) and ADS-HFSS simulated results of (a) output power and (b) DC component of the RF current delivered by the 300 GHz power-combined doubler. The simulations were performed using the SDD model considering a constant series resistance (red dots) and a RLC circuit (blue dots). The legend affects both figures.

Fig. 3.20(a) shows that the simulated model accounting for the RLC circuit seems to better fit the experimental results, mainly in the low frequency range of the band (similar results are obtained with and without RLC above the center of the band). However, it is very important to clarify that the capacitance C_E and inductance L_E values used for the RLC model have been artificially modified (an increased inductance L_E= 4.47 pH, 12 times higher than the theoretical value given by analytical equation 2.20, and a reduced capacitance C_E= 0.57 fF, 12 times smaller, following the rule of a constant $C_E L_E$ product). These results allow us to understand the impact of the RLC circuit in our LEC model of the PSBDs, but the values required to obtain a good agreement with the experimental results are not in good agreement with the analytical model proposed in the bibliography for the C_E and L_E values, probably due to the large signal conditions of operation of our PSBDs, where the theoretical small signal equivalent circuit is not valid.

In spite of the previously discussed problems, it is interesting to compare the results provided by constant series resistance R_S and the RLC models. First, they are equivalent in the high frequency range of the band, Fig. 3.20.(a), where the DC component of the current is very low, Fig. 3.20.(b), and the diodes work in a pure varactor mode. On the other hand, remarkable differences appear when working in the low frequency range of the band, where

the optimal conversion efficiency predicted by the RLC model is higher. This is because the PSBDs work in a non-pure varactor mode, as evidenced by the high values of the DC component of the current in RF conditions. The voltage applied to the PSBDs reaches values close to flat band conditions where additional non-static phenomena arises and the constant series resistance model appears to be not accurate enough. However, there are too many inconsistencies that hinder the validation of the small signal RLC equivalent circuit implemented in this study. First, the agreement with the experimental DC current is not better than that obtained with the constant series resistance model. Second, the study carried out in Fig. 3.6 demonstrates the sensitivity of the experimental results at the low frequency side of the band to the mechanical mounting of the MMICs, so that a better agreement with the experiments in this range is not very significant. In fact, the opposite behavior was observed in another mounted device (Figs. 3.8, 3.10, 3.11 and 3.12 at low frequencies), in which the predicted output power was overestimated by the constant series resistance model.

We can conclude with this analysis that, once again, the improved SDD capacitance model of PSBDs is able to closely approximate, using well-founded physical parameters, the harmonic generation of the devices, the optimal bias and the DC component of the current in RF conditions in most of the frequency band. Regarding the constant series resistance or RLC models, it is possible to conclude that the influence of possible frequency dependent series impedance is much smaller than the impact of the contribution of two-dimensional phenomena to the capacitance of the diode (as observed in section 3.1.4). However, the RLC model can improve the results of the simulation of the second harmonic generation. Additionally, a variation of the performances has experimentally been observed at the low frequency edge of the band in different 300 GHz doubler devices. For these reasons, it is not possible to identify any advantage using the RLC model, especially when defining the PSBDs epilayer properties for a new hypothetical application.

3.3 Conclusions

The development of a 300 GHz doubler for the LO chain of a 600 GHz receiver has been achieved. This doubler, presented in section 3.1.1, is able to manage up to 50-60 mW of input power with conversion efficiencies around 20-23 %. A dedicated experimental test bench was proposed for this frequency doubler with the aim of validating the developed SDD physical model of the PSBDs. The usefulness of the developed model has been demonstrated in section 3.1.4 where a comparison with the integrated ADS standard model of PSBDs has been carried out. Improved prediction capabilities of the diodes response have been demonstrated in this doubler application. The prediction capabilities of the optimal bias, the DC component of the current in RF conditions and the output power have been demonstrated using the extended SDD model in the ADS-HFSS simulations. The 300 GHz doubler chip design has been repurposed on the design of a power-combine doubler, presented in section 3.2, at the same frequency range of 270-320 GHz with the aim of being part of the multiplication LO chain of the 1.2 THz channel. The design of a 90 degree quadrature hybrid coupler has been detailed in section 3.1.1, and the final design of this power combine doubler has been presented in section 3.2.2. This doubler is able to manage up to 100-120 mW of input power featuring a conversion efficiency slightly improved around 23-25 %. The experimental results have been compared with ADS-HFSS simulations in section 3.2.5 using the developed SDD model, where an excellent agreement has been noted between this study and the previous results discussed for the single chip version of the doubler. The small signal RLC equivalent circuit has been taken into account in the analysis of different 300 GHz frequency doublers available during this work. However, no clear advantages have been noticed in the way it has been implemented due to the small influence of this additional dynamical element in the global performances of the device. Additionally, the deviation of the doubler performances at the low frequency edge of the band is higher between different mounted devices than the modification introduced by the RLC model.

4 A 600 GHz Frequency Doubler

The development of a 600 GHz frequency doubler is presented in this chapter. It was proposed by LERMA as part of the LO chain dedicated to the 1.2 THz receiver for the SWI project. A first design with two PSBDs developed at LERMA in 2014 and fabricated by LPN at the end of 2015 is presented in the first section. A redesign of this doubler has been proposed by the author of this work, resulting in improved device performances. The initial design is based on two anodes while the design proposed by this author uses four anodes with an improved epilayer topology. This second design was proposed as alternative to increase the available power for pumping the 1.2 Thz mixer since this design can handle higher input power and perform higher conversion efficiency. The first design is briefly described in the first section of this chapter while the second device, entirely developed as part of this doctoral work is thoroughly detailed in the second part.

4.1 Two-Anodes 600 GHz two Anodes Frequency Doubler

4.1.1 Virtual Device

The development of the virtual design was carried out in 2014 by Dr. F. Yang from the State Key Lab, Nanjing, China. This multiplier is based on the design of the 300 GHz doubler presented in section 4.1 and uses similar PSBDs, with the same layer structure but with a lower anode surface. Also, the dimensions of the waveguides, the chip and the number of diodes (2 anodes) have been adapted to different frequencies of operation (input frequency from 270 to 320 GHz).

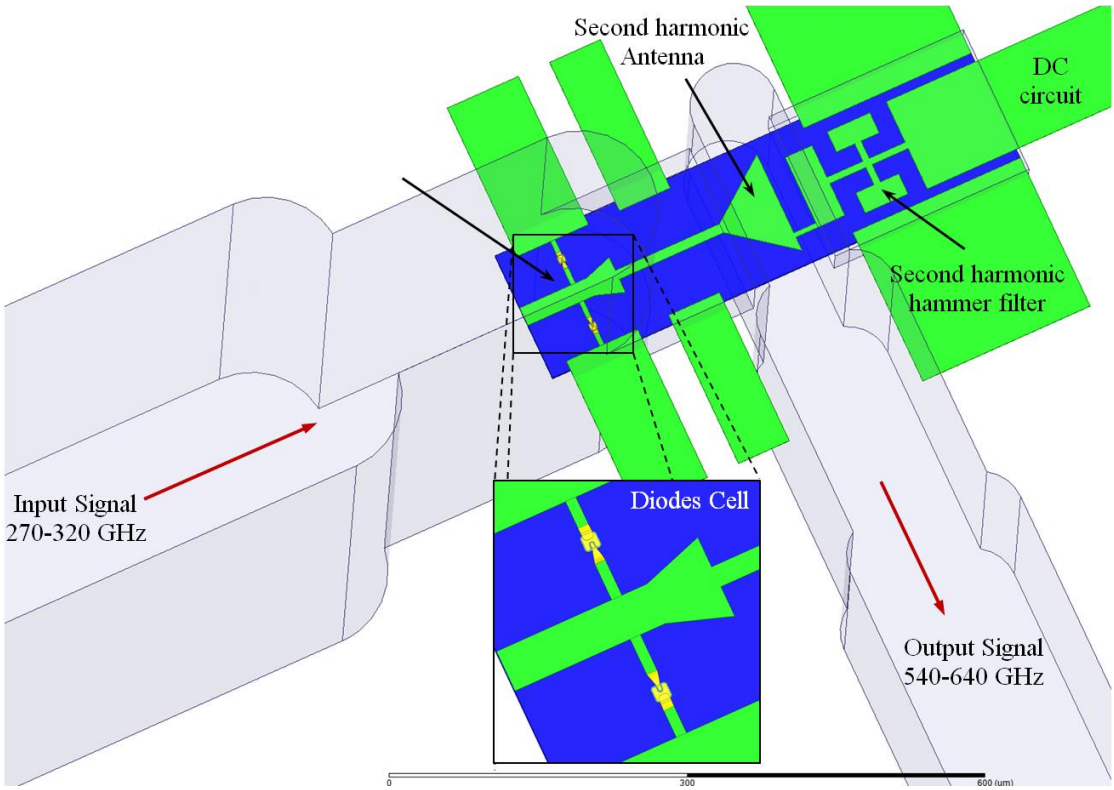

Fig. 4.1. HFSS 3D design of the two-anodes 600 GHz frequency doubler where the different parts of the MMIC chip are indicated. The balanced configuration of Schottky diodes is shown in a zoom. A hammer filter is used to block the exit of the second harmonic signal through the DC bias circuit.

The MMIC chip features an anti-series set of two planar Schottky barrier diodes integrated within the suspended microstrip circuit on a 5 μm-thick GaAs membrane placed in a split mechanical block by metallic beam-leads. The diodes are in a balanced configuration in such a way that the odd harmonics are generated in opposite phase by each branch of the diode cell while the even harmonics are generated in phase. It results in odd harmonics cancellation leading to a simpler and more compact design where only even harmonics are propagated in the chip. The virtual design is presented in Fig. 4.1, where all the elements of the microelectronic circuit are indicated. The input LO signal reaches the MMIC chip through a waveguide whose height (864 μm) is specifically designed to transmit the TE_{10} mode at the input frequency signal range. The thickness of the waveguide is chosen to cut off the TM_{11} mode that can potentially be coupled with the second harmonic generated by the diodes. The input structure of the MMIC is designed for coupling the diode cell with the TE_{10} mode transmitted within the input waveguide. The generated even harmonics are then propagated in a quasi TEM transmission line mode to the output stage of the MMIC chip by an intermediate channel which separates the input and output waveguides. A high-low transmission hammer filter optimized for cutting off the second harmonic is used to avoid losses of the desired signal in the DC circuit which is connected to a SMA connector in the mounted device.

The 600 GHz doubler chip was optimized for 4.5 mW of LO power per diode, i.e., the full chip is optimized for ~10 mW of LO input power between 260 – 320 GHz. The epilayer is doped at $1 \cdot 10^{17}$ cm^{-3} with a 350 nm thickness, the same as the one used for the 300 GHz doubler chip, but with an anode surface of about 1/5, each diode is ~3.5 μm^2, which results in a junction capacity $C_{j0} \approx 4.3$ fF (using eq. 2.21). The anode size has been chosen considering a nominal input power of ~4.5 mW, and accounting for the epilayer doping level, the epilayer thickness and the frequency range. A 21 Ω series resistances was considered in the development of this device, following the experimental rule of a constant product $C_{j0} \cdot R_S$ (and knowing the experimental results of the PSBDs used for the 300 GHz doubler).

4.1.2 Mechanical Block

The design of the mechanical block can be now defined according to the dimensions obtained during the matching network optimization. Since this 600 GHz doubler has been especially developed for the 1.2 THz receiver proposed by LERMA-LPN-CNRS for the SWI project, the mechanical block where the 600 GHz doubler chips are mounted needs to correctly align the 300 GHz doubler block with the 1.2 THz mixer block while having a design as compact as possible. The principal consideration applied in this design is reducing the 600 GHz signal path as much as possible since the transmission losses increase with the frequency. The first version of the LERMA's 600 GHz doubler block is presented in Fig. 4.2, where all the elements of the block have been indicated.

The input signal enters in the 600 GHz doubler block from the 300 GHz power-combined doubler presented in section 3.2 while the output signal comes out of the device to the 1.2 THz mixer in a perpendicular configuration with respect to the input signal. A 45º bending section has been defined at the input and output waveguides, whose geometry has been optimized through HFSS simulations in order to avoid any power loss of the transmitted signals. It is also possible to comment in Fig. 4.2 that the output path (~ 2 mm) is much

shorter than the input path (~10 mm) in order to reduce the transmission losses inside the block. The 90º angle configuration between the input and the output signals emerges from the requirements of the SWI optical path configuration and the 1.2 THz mixer block design proposed by LERMA to correctly align the 1.2 THz receiver and the optical path of the 1.2 THz signal.

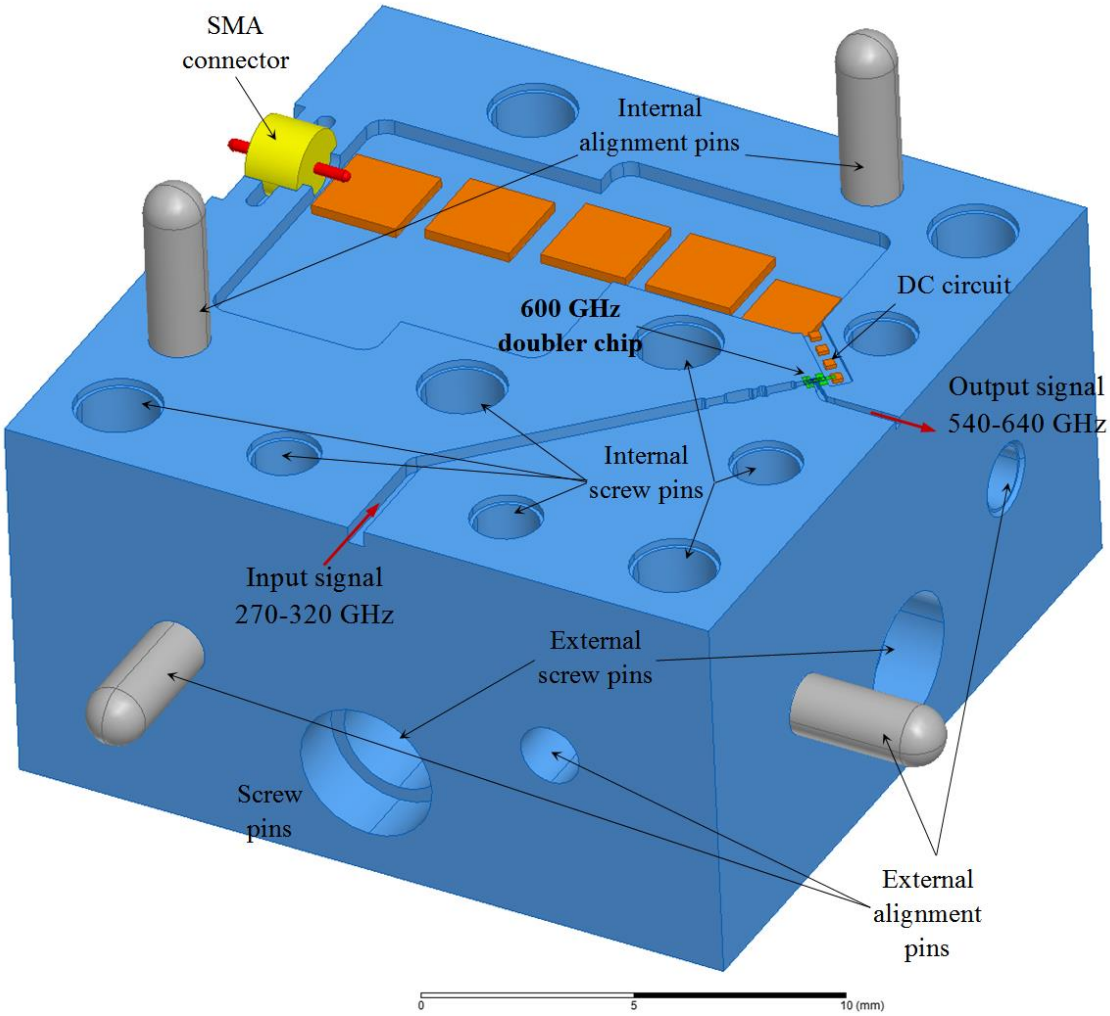

Fig. 4.2. 600 GHz block designed for the two-anodes doubler chip. The different elements of the half block have been indicated. The dimensions of the block are 19x19x20 mm^3.

A larger number of screws are used in the 600 GHz block design to ensure the correct alignment and closure of the block to avoid any leak of signal between the split blocks. However, the precision of the block fabrication process starts to be a critical point at this level, since some critical dimensions of the MMIC are in the 20-50 µm range while the precision of the block fabrication process is usually ±10 µm. This may have an impact on the mounting process, where any defect of the block geometry is superimposed to the possible misalignments when placing the MMIC. The precision also affects the external and internal alignment pins, mainly at the output of the 600 GHz doubler block, since the waveguide section is 216x432 $µm^2$ and a misalignment between both parts of the block may significantly affect the waveguide geometry. The DC circuit consists of several capacitors (not grounded) used to bonding the SMA connector to the MMIC chip. The SMA connector is a semi-

precision coaxial RF connector with a 50 Ω impedance specifically designed for signals from DC to 18 GHz.

4.1.3 Experimental Device

The ensemble of the experimental development of the two anodes frequency doubler is presented in Fig. 4.3. The images of the fabricated mechanical block together with the image of the fabricated chips, before releasing them from the wafer and the already mounted chip, highlights the ensemble of the fabrication process developed by LERMA-LPN-CNRS.

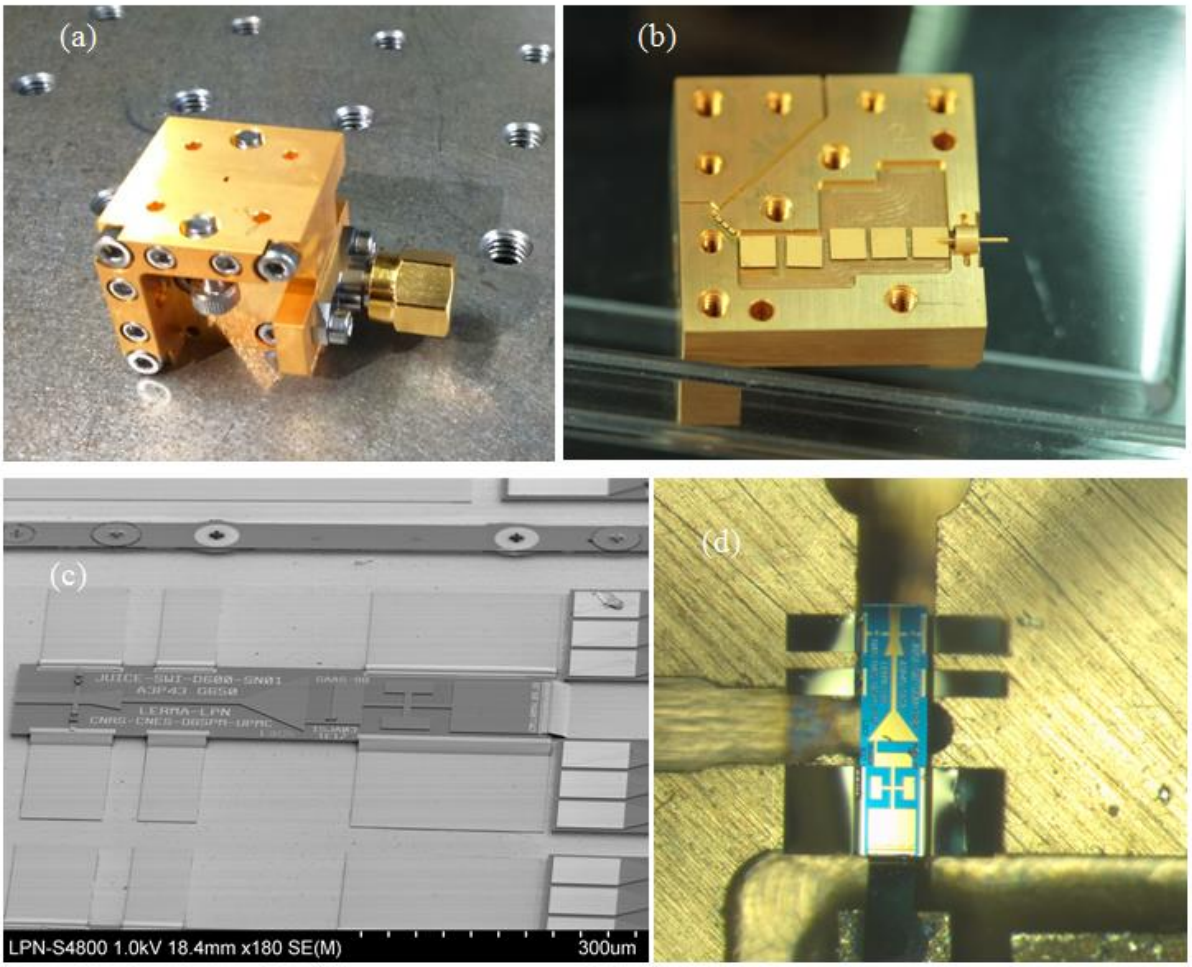

Fig. 4.3. (a) and (b) Photographs of 600GHz doubler block fabricated by SAP-micro before assembly. (c) Photography of the MMIC chip of the 600 GHz two anodes doubler fabricated by LPN before releasing them from the wafer. (d) MMIC chip at 600 GHz mounted in the mechanical block.

Once the chip is mounted in a mechanical block it is safe to perform the measurement of the I-V characteristic of the diode cell. This measurement is the easiest way to monitor the state of the PSBDs and their symmetry in the balance configuration of the diodes structure. In this case there are two branches with only one diode, thus the I-V measurement of the average performance of each diode can be obtained dividing by two the measured current, since the same applied bias falls in each diode and it does not need to be corrected.

4.1.3.1 Experimental I-V Characteristics

The measured I-V characteristics of the individual PSBDs used in the MMICs of the 600 GHz doubles, presented in Fig. 4.4, allows also defining the physical model of the diodes used in ADS-HFSS simulations. The most important parameters, as previously discussed in the second chapter, are the DC series resistance R_S, the ideality factor η, the built-in voltage V_B and the saturation current. Together, this allows us to define the I-V and the C-V characteristics of the simulated diodes with the aim of approximating them as much as possible to the real PSBDs. As a consequence, a saturation current I_S= 2.0·10^{-12} A, an ideality factor η= 1.29, a built-in voltage V_B= 0.73 V and a DC series resistance R_S= 26 Ω are obtained when fitting with the analytical model presented in section 2.2.

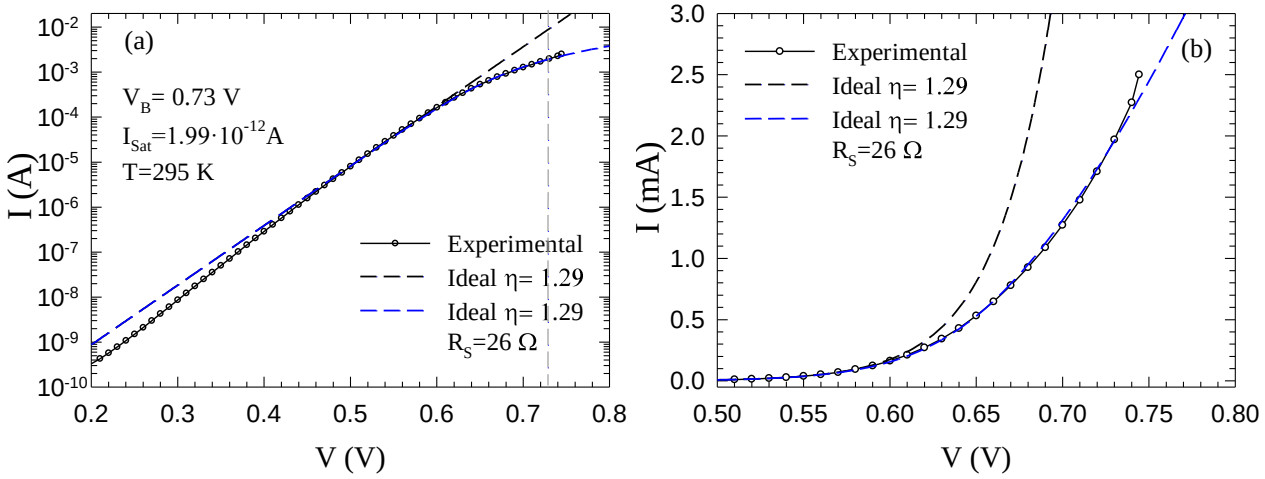

Fig. 4.4. I-V characteristic of the PSBDs of the fabricated two-anodes 600 GHz doubler mounted in the SN01 block in (a) logarithmic and (b) linear representation. The physical parameters of the diode are calculated by fitting the experimental results (black dots) with the analytical model (dashed blue line).

The measurement of the I-V characteristics of several two-anode chips show that the built-in voltage is always in the range 0.69-0.73 V, slightly lower than expected when comparing it with the PSBDs of the 300 GHz doubler (using exactly the same epilayer doping and thickness), where it was around $V_B \approx$ 0.78 V. This reduced built-in voltage does not dramatically affect the final performance of the 600 GHz doubler, unless it is over-pumped, since it only affects the optimal bias voltage. The determination of the ideality factor is not as clear as it was in the results presented in Fig. 3.4 for the 300 GHz doubler, because the exponential part of the I-V characteristic is not as ideal as expected. It results in an ideality factor that depends on the considered current range, and it varies from 1.18, if it is calculated between 1 nA to 1 µA current range, to 1.29 if it is calculated using the current range above 1 µA. However, if the 1.18 ideality factor is considered in the analytical equation, it is not possible to correctly fit the upper region of the I-V characteristic while it can be correctly fitted if the higher currents are prioritized. The ideality factor η= 1.29 is considered the most adequate value to fit the experimental results presented in Fig. 4.4, since it accurately fits the I-V characteristic above 1 µA. Additionally, the RF response of the multipliers is principally determined by the C-V characteristic, while the I-V model is especially important when the excited signal in the PSBD approaches the built-in voltage. Regarding the series resistance, the values measured in different chips are in the range 24-26 Ω, which is around 3-5 Ω larger than expected according to the experimental rule $R_S C_{j0}$= Const. This deviation can be mainly

associated to a deviation in the fabrication process with respect the fabrication run of the 300 GHz doubler. It is because the PSBDs topology is the same, where the only difference is the anode size reduction that should be reasonably accounted for by the $R_S C_{j0}$ relationship.

The analysis of the I-V characteristics of the diodes used for the fabrication of this run of 600 GHz doubler chips, allows us to conclude that some kind of disruption appeared in the fabrication process of these PSBDs, since the previous fabrication process of the 600 GHz mixer presented by LERMA in [Treut15] presented more ideal I-V characteristics while featuring an anode surface seven times smaller. However, this does not have a negative impact in the performance of our frequency multipliers, where a good junction capacitance and a low series resistance are the key properties.

4.1.3.2 Experimental RF Results

The measurements of the 600 GHz doubler were carried out after the measurements of the 300 GHz power-combined doubler presented in Fig. 3.19. Unfortunately, several deviations have been identified in the mechanical block dimensions fabricated by RPG. The output waveguide is up to 10 µm wider than the nominal one (91 µm), and the middle channel is also around 10 µm larger than the nominal one (87 µm). These deviations are not negligible compared with the nominal dimensions of the mechanical block. It has an impact in the centering of the frequency band and it introduces an additional difficulty in the placement of the chip, since the deviation presented by the waveguide matching network system affects the coupling of the input power in the diode cell. However, similar performances should be obtained along the frequency band. The experimental test bench used to characterize the 600 GHz doubler performance is presented in Fig. 4.5, where the additional elements are indicated.

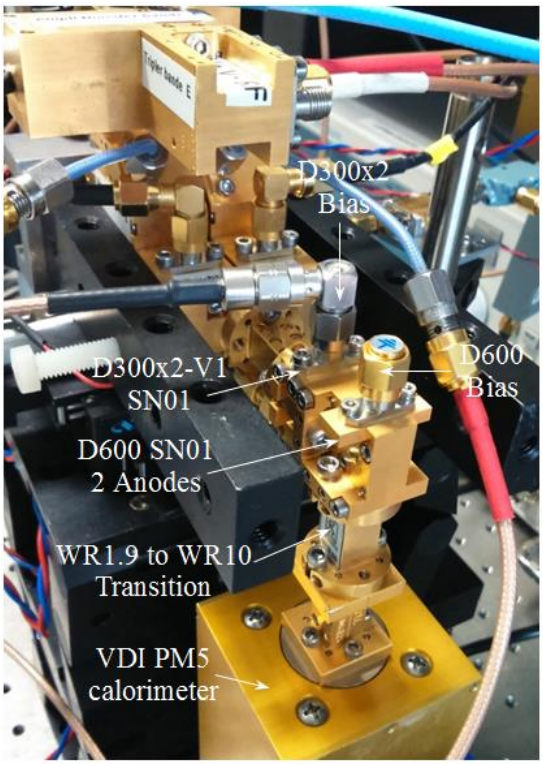

Fig. 4.5. Test bench used to characterize the 600 GHz doubler using the RPG DM driver chain developed for the 1.2 THz channel and the 300 GHz power-combined doubler. The different elements have been indicated.

The 600 GHz doubler is connected directly after the 300 GHz power combine doubler characterized in section 3.2.4.1, but a transition waveguide from WR1.9 to WR10 is now required to match the 600 GHz doubler output signal with the VDI PM5 calorimeter. Non-negligible standing waves appear in this setup due to the proximity between the 300 GHz and the 600 GHz doublers. The experimental output power delivered by the 600 GHz doubler is shown in Fig. 4.6. The bias of the 600 GHz doubler has been tuned to find the best output power performance, while the 300 GHz power-combined bias has been fixed at the same values used in Fig. 3.19. A bias between -0.5 V and -3 V was required along the frequency band, but the average bias is between -1 V and -2 V, as indicated in Fig. 4.7. The input power

delivered by the 300 GHz power combine doubler (dashed red lines) is the same one measured in Fig. 3.19 but a 0.3 dB gain has been introduced to correct the losses associated with the transition WR3.4 to WR10 used in Fig. 3.10. Transmission losses around 0.3 dB are also estimated in the transmission waveguide from WR1.9 to WR10 in Fig. 4.5. The conversion efficiency has been calculated with the quotient of the measured delivered power by the 600 GHz doubler and the 300 GHz power combine doubler when considering a 0.3 dB gain in each case, in order to correct the transmission losses in the PM5 calorimeter.

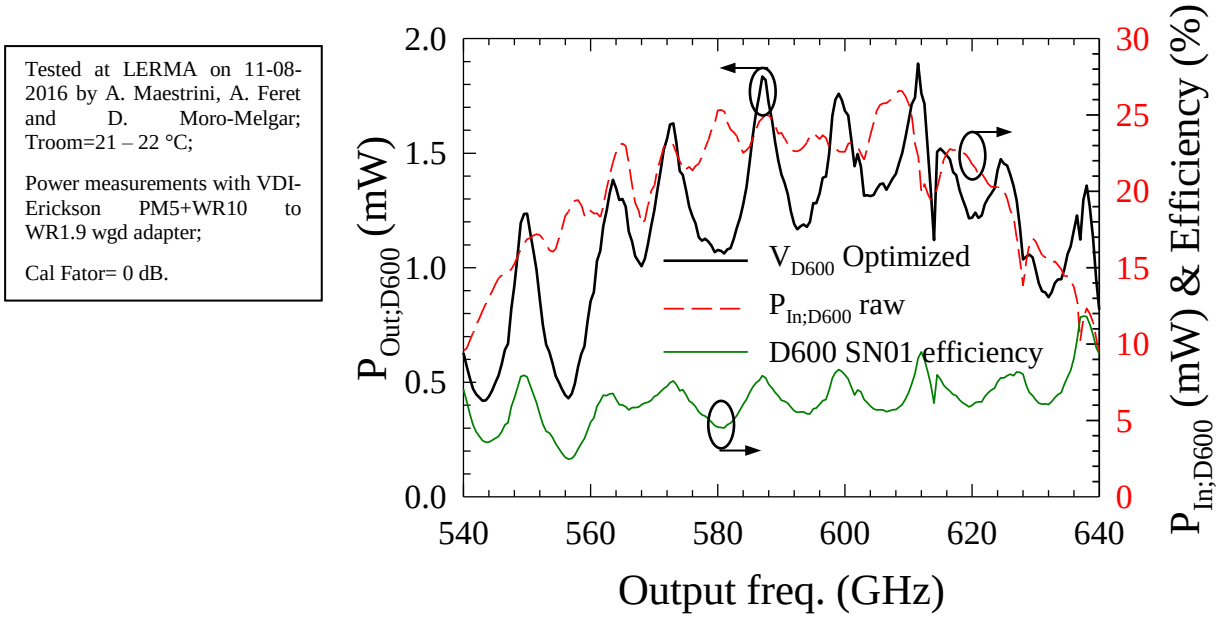

Fig. 4.6. Experimental output power (black line) delivered by the 600 GHz doubler when pumping it with the 300 GHz power combined doubler presented in Fig. 3.19 (whose power is shown with the dashed red line). The conversion efficiency is also plotted (green line).

It is worth highlighting the strong influence of the standing waves on the 600 GHz doubler performance along the frequency band, especially at the low frequency edge. It is normal to have a more sensitive LO coupling at the low frequency range of these MMIC doubler designs. The reflected power at the input of the 600 GHz doubler will then be reflected at the output stage of the 300 GHz, generating additional standing waves. The conversion efficiency plotted in Fig. 4.6, allows estimating how the input power is deviated from the nominal value given by the dashed red line. It indicates an efficiency that oscillates between a 5 % and 8 %. It will be demonstrated in next sections that the way the delivered output power by the 300 GHz doubler is modified by the standing waves, does not strongly modify the global efficiency. It means that the real efficiency does not oscillate as much as it does in Fig. 4.6 because the oscillations in the 600 GHz doubler output power are associated with a reduction of the input power by the standing waves. It will result in a conversion efficiency between a 6 % and 7 % along the band.

The impact of the bias on the previously observed standing waves has been analysed in this experimental setup by fixing the bias of the 600 GHz doubler while keeping the optimized voltage values for the 300 GHz power combined doubler. The results are plotted in Fig. 4.7, where the measurements of the output power delivered by the 600 GHz doubler have been

carried out when fixing its bias at -1.5 V, -1.8 V and -2.1 V (values in the range of the optimal voltages found along the frequency band).

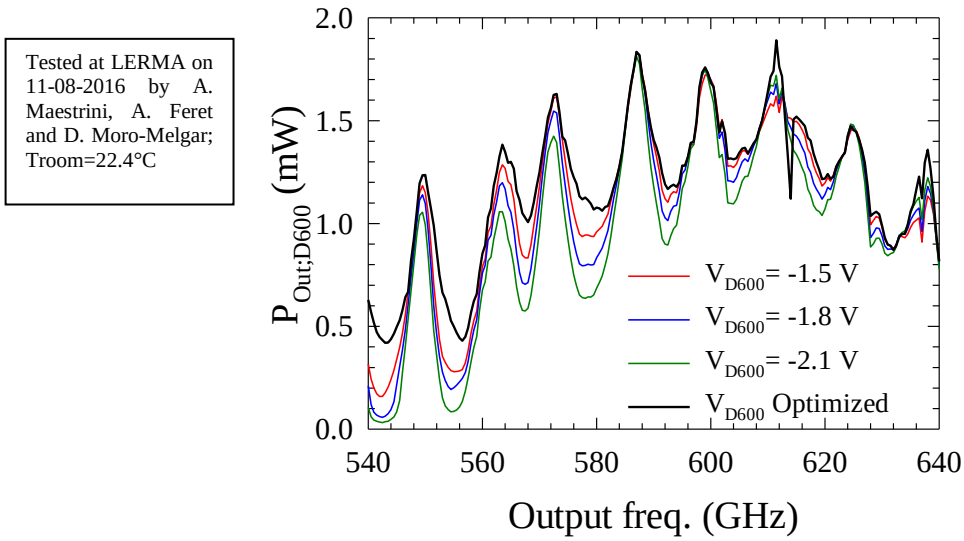

Fig. 4.7. Optimum experimental output power (black line) delivered by the 600 GHz doubler compared with that delivered when fixing the 600 GHz doubler bias at -1.5 V (red line), -1.8 V (blue line) and -2.1 V (green line).

Interesting results are obtained at several frequencies of the band. First, similar performances are obtained around some of the peaks of the frequency response (i.e. 587 GHz, 598 GHz and 624 GHz) from -1.5 V to -2.1 V. Second, less reverse biases are better in order to obtain the maximal performance in the lower half of the band (<590 GHz) while more reverse biases are suitable to maximize the performance in the upper half of the band. Finally, a low reverse bias is more adequate to maximize all the minimums found in the experimental performance at 542 GHz, 555 GHz, 567 GHz, 580 GHz, 592 GHz, 604 GHz, 619 GHz and 631 GHz. It indicates the presence of standing waves with a frequency around 10-12 GHz. It will be demonstrated in next sections that the optimal performance, given by the black line in Fig. 4.7, is a trade-off between the 600 GHz doubler bias tuning to maximize its conversion efficiency and the impact of this bias on the effective input power delivered by the preceding multiplication stage. It is possible to recognize in Fig. 4.7 that the minimums of the optimized output power correspond with a lack of input power from the 300 GHz doubler, due to the influence of the standing waves, which can be mitigated by reducing the 600 GHz doubler bias in order to better take advantage of the non-linearity of the PSBDs capacitance. Regarding the maximums of the experimental output power, they are also associated with an increment of the input power due to the standing waves, but this increment strongly depends on the 600 GHz bias.

We conclude this RF analysis with a 600 GHz LO chain able to deliver more than 1 mW in most of the band, but the strong interaction between the 300 GHz and 600 GHz doublers leads to strong oscillations of the available output power, especially in the low frequency range. The only way to correctly compare the experimental results with the ADS-HFSS simulations is accounting for the 300 GHz and 600 GHz doubler in the same simulated test-bench in order to analyse the interaction mediated by the standing waves. However, this analysis is limited

by the fact that the standing waves at the output stage of the 300 GHz doubler will also induce unknown variations of the coupling performance at its input.

4.1.4 Simulations of the Two-Anodes 600 GHz Frequency Doubler

This section is dedicated to the comparison of the experimental results presented in Fig. 4.6 with the predicted performances in the ADS-HFSS test-bench of the 600 GHz doubler. Additionally, a comparison of the predicted results between the developed SDD model and the ADS standard STD model is carried out. The 600 GHz doubler is simulated without being connected to the 300 GHz doubler in this section and is ideally pumped with the experimental power values obtained for that block (Figs. 3.19 and 4.6). It means that no standing waves appear. The parameters for the simulations are based on the values obtained in Fig. 4.4: $I_{Sat}= 2\cdot10^{-12}$ A, $\eta=1.29$ and $V_B= 0.73$ V. The series resistance will be adjusted in order to correctly reproduce the experimental conversion efficiency of the block. It is important to mention that the simulations of PSBDs with $1\cdot10^{17}cm^{-3}$ epilayer doping, made in [Graj00b] considering an input frequency range 270–320 GHz and average bias between -1 V and -2 V, shows that saturation phenomena appear in the carrier transport mainly at high reverse bias. It means that the results predicted by our LEC model are expected to lose accuracy as the reverse bias is increased.

The ADS-HFSS simulations using the standard STD and the developed SDD capacitance models of the PSBDs are compared with the experimental results, shown in Figs. 4.8 and 4.9, of the output power, the DC component of the current in RF conditions, the efficiency and the optimal bias of the 600 GHz doubler. In both cases we have used the same parameters for the analytical expression of the I-V curve, based on the experimental results, $I_{Sat}= 2\cdot10^{-12}$ A, $\eta=1.29$ and $V_B= 0.73$ V at $T=295$ K. The values of the series resistance that has been found to be adequate to fit the experimental results are $R_S=29\ \Omega$ (3 Ω higher than the experimental DC one, ~11 %) and $R_S=36\ \Omega$ (10 Ω higher than the experimental, ~38 %) in the case of the SDD and STD models, respectively. The additional parameters of the SDD model are $\alpha= 0.85$, W_{EP}-$W_{CA}= 48$ nm and W_{CB}-$W_{EP}= 9$ nm, while for the STD model we use is $\alpha= 0.6$.

The optimal bias used experimentally to optimize the output power delivered by the two-anode 600 GHz doubler, Figs. 4.8(d) and 4.9(d), is in the range -0.5 V to -1.5 V in the lower side of the frequency band and approximately between -1.2 V and -2.5 V for the higher frequencies. The strong reverse bias (-3.7 V) experimentally obtained at 614 GHz is not a valid measurement since, as shown in Fig. 4.7, the output power is higher at -1.5 V. Also, the strong bias (-4.7 V) used at 612 GHz to obtain the highest value of output power measured in this device seems to be also anomalous since not only strong saturation phenomena should appear for such a high reverse bias, but the voltage excited in the diode would largely exceed the breakdown voltage ($V_{BR}\approx$ -8 V). In order to simplify the study, the ADS-HFSS simulations have been performed by fixing the 600 GHz doubler bias at different values between 0.5 V (near the optimum bias at the lower range of the frequency band) and -2 V (optimum for the higher frequencies). In fact, the simulated output power increases as the reverse bias increases, Figs. 4.8(c) and 4.9(c), regardless of the SDD of STD models used. This happens because this two-anode 600 GHz doubler was optimized for an input power

level of 10 mW but we are pumping it much more power (up to twice this value, see Fig. 4.6), so that the epilayer is fully depleted at low reverse bias (its thickness is too small). Therefore, the experimental optimal bias is strongly determined by the breakdown voltage of the diodes, which is reached when biasing between -2.5 V and -3 V, but this is not accounted for in these simulations.

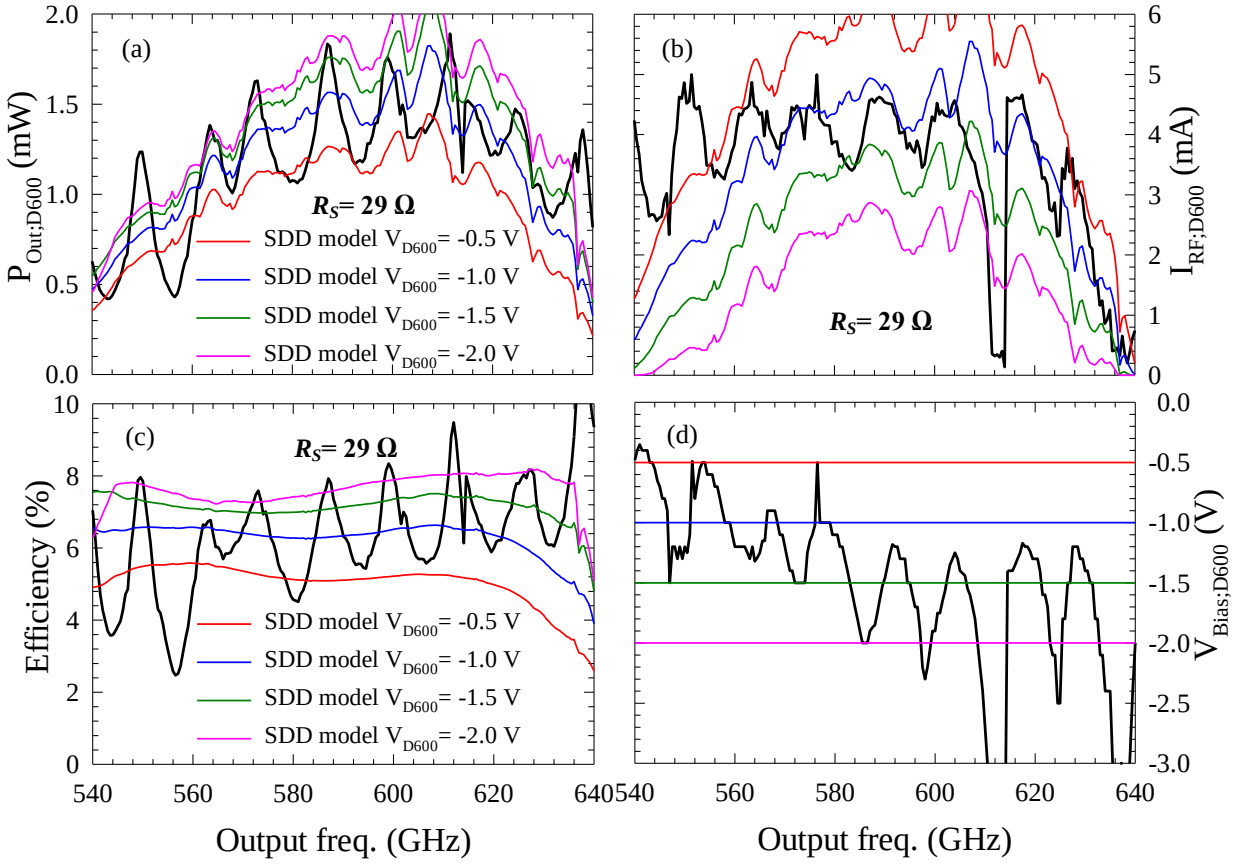

Fig. 4.8. Comparison between ADS-HFSS simulations using the developed SDD model of the PSBDs and experimental results (black lines) of (a) output power, (b) DC component of the current in RF conditions, (c) conversion efficiency and (d) operating bias of the 600 GHz doubler. The simulations have been performed at fixed bias points of -0.5 V (red lines), -1.0 V (blue lines), -1.5 V (green lines) and -2 V (pink lines). The value for the simulated series resistance is R_S= 29 Ω, which provides the best agreement with the experimental results. T= 295 K.

It is important to note that the 600 GHz doubler is individually simulated using the input power given by the measurements of Fig. 4.6, thus no standing waves modify the doubler performances. Apart from the fact that the simulations do not show the strong oscillations associated to the standing waves observed in the experiments, a very good agreement between the predicted output power and the experimental one is obtained, both with the SDD and the STD models. Regarding the conversion efficiency, Figs. 4.8(c) and 4.9(c), it ranges from ~5 % to ~7 % in the lower half of the frequency band and from ~7 % to ~8 % in the higher. Regarding the DC component of the current in RF conditions, Figs. 4.8(b) and 4.9(b), the experimental results are reasonably reproduced by the simulations performed for biases near the optimal value at each frequency. This result could be improved by slightly reducing the simulated series resistance, but at the expense of an overestimation of the output power and efficiency of the MMIC. The expected influence of saturation phenomena, not taken into

account in our models, is a reduction of the conversion efficiency when increasing the reverse bias, i.e., the results of the simulations shown in Figs. 4.8 and 4.9 for -1.5 and -2.0 V should be closer to those obtained with -1.0 V. It is because the saturation phenomena induce a reduced swing of the depletion region depth during one period of the LO signal [Pard12].

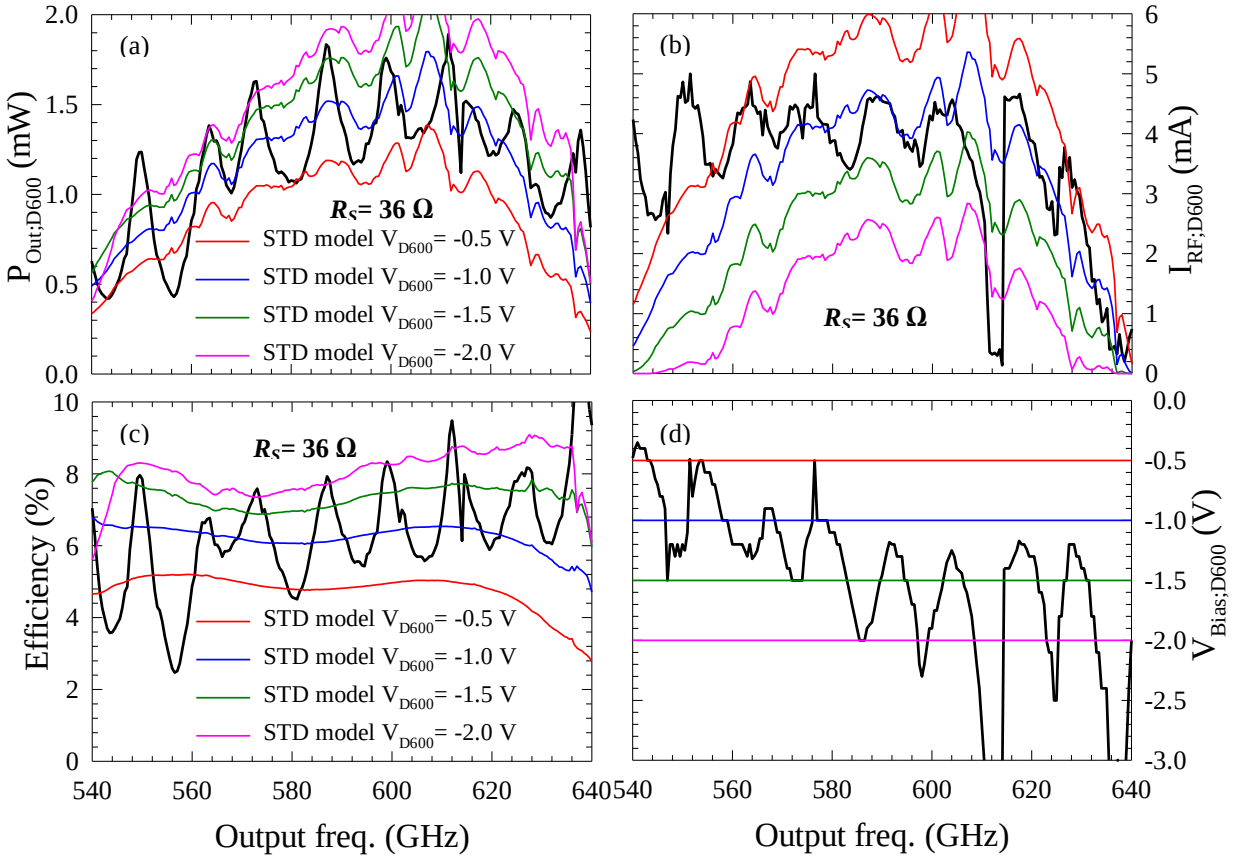

Fig. 4.9. Comparison between ADS-HFSS simulations using the STD model of the PSBDs and experimental results (black lines) of (a) output power, (b) DC component of the current in RF conditions, (c) conversion efficiency and (d) operating bias of the 600 GHz doubler. The simulations have been performed at fixed bias points of -0.5 V (red lines), -1.0 V (blue lines), -1.5 V (green lines) and -2 V (pink lines). The value for the simulated series resistance is R_S= 36 Ω, which provides the best agreement with the experimental results. T= 295 K.

Regarding the series resistance used for the simulations, we have to use higher values than the one obtained from the I-V curves of Fig. 4.4. Within the SDD model, the value used, R_S=29 Ω, is still in an acceptable range of deviation, since an increase of 1-2 Ω in the experimental resistance with respect to its DC value can be expected when applying RF conditions [Tang10]. Also, self-heating could be responsible for additional variations of the series resistance. If a rise in the temperature of operation of the diodes between 30 to 40 K is considered in the simulations, the series resistance has to be reduced in 1-2 Ω in order to obtain results similar to those of Fig. 4.8. This means that the difference between the measured DC series resistance and the value used in the simulations with the SDD model is within a reasonable range that can be explained when accounting for an additional dynamic resistance and diode self-heating in RF conditions. On the other hand, when using the STD model, the value of the series resistance that allows a correct agreement with the experiments is much higher R_S=36 Ω. This significant increase is necessary to counteract the overestimation of the conversion efficiency of the diodes that provides the STD model due to

an undestimated value of the capacitance. This is a non-physical artificial consideration that allows improving the agreement with the measurements.

The results of this analysis explain very clearly that a good doubler can be designed using a very simple model, such as the STD, even if it does not take into account important physical phenomena. However such model does not allow defining an accurate process to extrapolate the predictions because it is not possible to know the values of the model parameters that fit the experimental results until it is experimentally characterized. The only correct prediction the STD model allows in varactor mode affects any new design where the frequency range and diodes properties are similar to a previously fabricated design. However, it does not allow an adequate definition of the properties of the PSBDs (anode surface, epilayer doping and thickness, etc.) when facing a change in the power level or frequency range of the desired application.

4.1.5 Experimental Comparison with Combined Simulations of the 300 GHz Power-Combined and 600 GHz Doublers

The 300 GHz power combine doubler and the 600 GHz doubler are simultaneously simulated in this section in order to shed light on the interaction between multiplication stages mediated by the standing waves. Since we don't have the design of the RPG 150 GHz doublers, the simulated input signal in the 300 GHz doubler is fixed in accordance with results given by the red dashed line in Fig. 3.19. However, the experiments show that the standing waves generated between the input stage of the 600 GHz doubler and the output stage of the 300 GHz power combine doubler are able to affect how the input stage of the 300 GHz doubler interacts with the incoming signal generated by the RPG source, i.e., fixing the input power in the 300 GHz simulated doubler induce a constraint in the final result, possibly modifying the standing waves generated when the 600 GHz doubler is connected to the whole chain.

The first analysis presented in Fig. 4.10 represents how the output power delivered by the 300 GHz power combined doubler is modified when connecting the 600 GHz doubler and how it affects the final output power delivered by the 600 GHz doubler. The SDD model will be used and the parameters of the PSBDs for the 300 GHz doubler are the same as those used in Fig. 3.20, i.e., I_{Sat}= 2.59·10^{-13} A, η= 1.18, C_{j0}= 19.7 fF, V_B= 0.765 V, T= 295 K and series resistance R_S= 5.2 Ω. This means that the output power obtained in the simulations of the 300 GHz doubler in the lower half of the band is smaller than the experimental one, Fig. 3.20, but this fact does not affect the main conclusions of this study. For the 600 GHz doubler we use the same parameters as in section 4.1.4 for the SDD model of the PSBDs, i.e., I_{Sat}= 2·10^{-12} A, η=1.29, V_B= 0.73 V, T=295 K, α= 0.85, β= 0.64, W_{EP}-W_{CA}= 48 nm and W_{CB}-W_{EP}= 9 nm with R_S= 29 Ω. The input power and the optimum bias of the power combined 300 GHz doubler is fixed for each frequency using the experimental values, Fig. 3.20(a).

The output power delivered by the 300 GHz doubler simulated without connecting the 600 GHz doubler is given by the black line in Fig. 4.10(a). The results of the simulations when connecting the 600 GHz doubler biased at -0.5 V, -1.5 V and -2.5 V show how the connection of the 600 GHz doubler affects the power effectively delivered by the 300 GHz

doubler (input power of the 600 GHz doubler), producing the ripples evidencing the presence of such standing waves. Thus, the effective input power of the 600 GHz doubler is modified by its own polarization. This effect, at these levels of input power, is stronger for low (-0.5 V) or high reverse bias (-2.5 V) but it is not so evident at -1.5 V. It is also remarkable that the maximums induced by the -0.5 V bias correspond to the minimums at -2.5 V. This results in the important fact that at certain frequencies in the lower side of the band the highest effective input power [and also the maximum output power, Fig. 4.10(b)], is obtained when biasing at -0.5 V, in agreement with the experimental results of optimum bias shown in Fig. 4.8(d) and 4.9(d). We recall that when simulating the 600 GHz doubler alone the output power was monotonically increasing when increasing the reverse bias, so that it was not possible to obtain the optimum bias point to be compared with the experiments. On the contrary, the optimum bias of the 600 GHz doubler can be estimated with the simulation of the 300 GHz doubler at its input. Indeed Fig. 4.10(b) shows that the maximum output power results of the combination of the available input power and the efficiency of the diodes to generate the second harmonic at each bias.

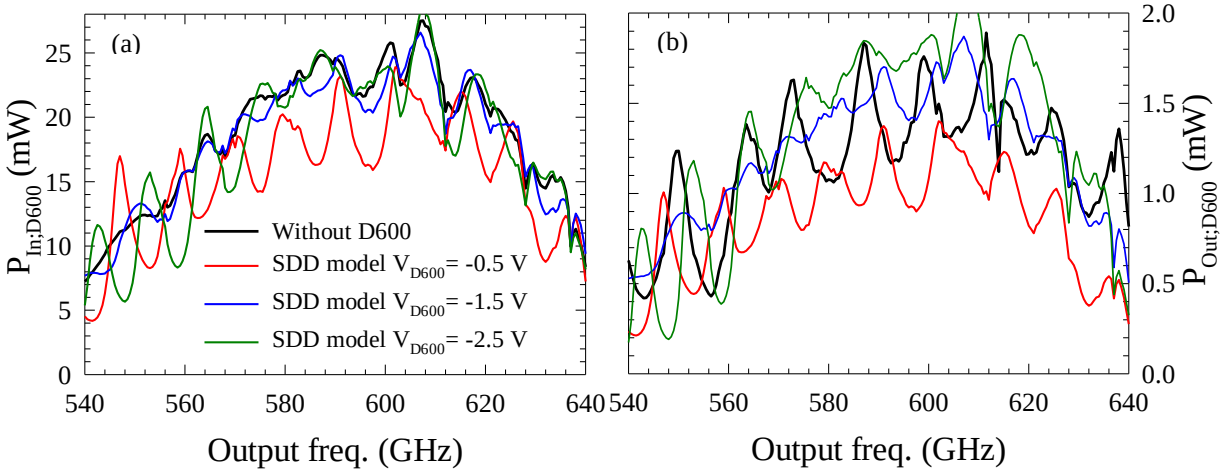

Fig. 4.10. Comparison between the simulated output power by (a) the 300 GHz power combine doubler without (black line) connecting the 600 GHz doubler and (b) the delivered power by the 600 GHz doubler when connecting it biased at -0.5 V (red line), -1.5 V (blue line) and -2.5 V (green line). The input power of the 300 GHz doubler is fixed with the values given in Fig. 3.19. The legend affects both Figures.

However, remarkable discrepancies can be observed between these simulation results and the experimental results presented in Fig. 4.7. The experimental oscillations are correctly predicted by ADS-HFSS simulations but they also predict a displacement of the maximums of the output power when sweeping the bias, not in agreement with the experimental behavior observed in Fig. 4.7. We attribute this discrepancy to the fact that the standing waves generated between the 600 GHz doubler and the 300 GHz doubler affect also the effective input power delivered into the 300 GHz by the RPG source. It is possible to extract this conclusion when analyzing the conversion efficiencies of each doubler, Fig 4.11. The first interesting point to note is the relatively flat conversion efficiency of the 600 GHz doubler, despite the strong variations of the effective input power, while the conversion efficiency of the 300 GHz doubler features the standing-wave related oscillations. This means that the modifications induced by the standing waves in the effective input power of the 600 GHz doubler are strongly related to the capacity of the 600 GHz doubler diodes to absorb the

incoming LO power. Both doublers were individually optimized to feature a flat coupling capacity along the band, but the presence of standing waves induces oscillations of the matching impedance of the diode cell around the optimized value. This results in an interaction with the standing waves along the band which induces variations in the input power of the 600 GHz doubler that keeps nearly constant the conversion efficiency of the doubler along the band. However, a fixed input power is artificially imposed on the 300 GHz doubler, so that the oscillations of the conversion efficiency featured by the 300 GHz doubler are associated with the way the standing waves modify PSBDs matching with both the input and output matching network.

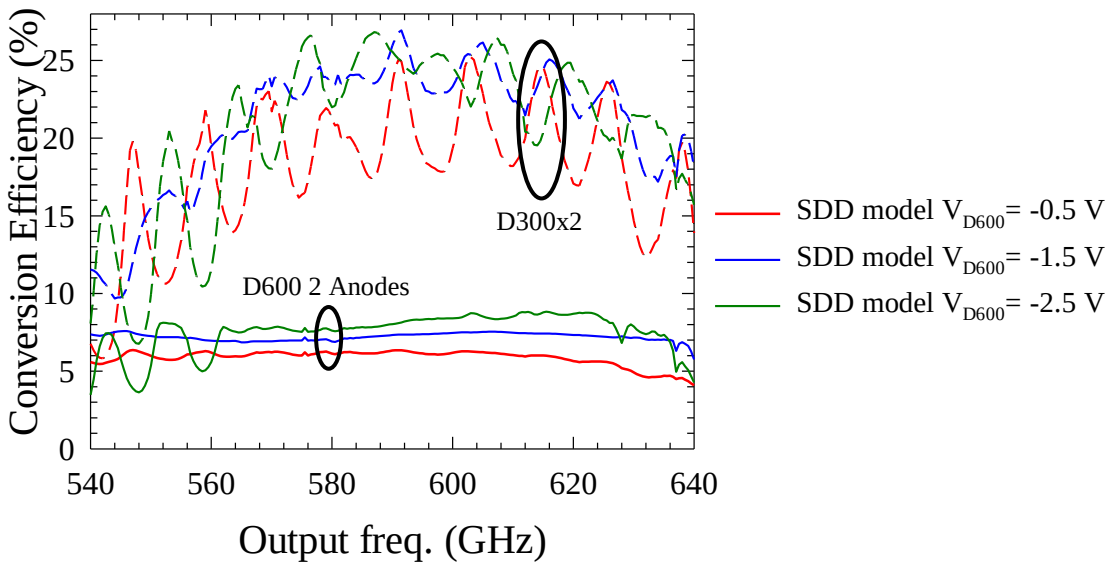

Fig. 4.11. Conversion efficiency obtained in ADS-HFSS simulations of the (a) 300 GHz power combine doubler and the (b) 600 GHz doubler when they are simultaneously simulated. A fixed set of input power and bias values are defined for the 300 GHz doubler in accordance with Fig. 3.19.

With these results we can conclude that the effective power delivered by the RPG source to the 300 GHz doubler should also be modified in a way that softens the effective conversion efficiency of the 300 GHz doubler plotted in Fig. 4.11.(a). In that way the constant position of the experimental maximums and minimums in Fig. 4.7 can be explained, since the coupling capabilities of PSBDs in the 600 GHz and 300 GHz doublers are jointly modified by the standing waves.

4.2 A 600 GHz four Anodes Frequency Doubler

A new version for the 600 GHz frequency doubler is proposed in this section. The optimization process of the PSBDs properties has been developed by this author based in the extended SDD model. The different stages of the development are detailed in this section. The key considerations for the PSBDs properties definition are initially discussed. Then, the design of each part of the MMIC chip is discussed indicating the simulation process in the ADS-HFSS test-bench. The predicted performance is finally discussed and compared under equivalent conditions with the previous version of the two anodes doubler.

4.2.1 Optimization of the PSBDs Properties

The conversion efficiency when changing the physical properties of the PSBDs is studied in this section. It is necessary to account for several dependencies that will finally define the suitable characteristics of the PSBDs considered in the applications. The final choice of the PSBD depends on the expected input power in each anode, the frequency range and the feasible impedance matching of the diode cell with the matching network of the MMIC chip. It is not possible in practice to consider all these dependences to carry out a direct optimization of the PSBD. It is more suitable to propose a few possibilities previously analyzed that will be tested during the design and optimization process. We focus this study on the variation of the epilayer characteristics of the considered PSBDs. All the additional variations and constrains which emerge from this modification are discussed and related with the fabrication techniques. I start by defining the new epilayer doping of the PSBDs. The main consideration when varying the epilayer doping is the variation induced in the breakdown voltage of the diode. Regarding the experimental knowledge obtained with the previous frequency doublers, the physical properties of the epilayer in both the 300 GHz doubler and the 600 GHz doubler are equivalent. The PSBDs features a 350 nm epilayer thickness doped at $1\cdot10^{17}$cm^{-3} where the anode size depends on the input power managed by each diode. These physical properties of the PSBDs and the fabricated diodes at LPN have demonstrated a breakdown voltage, $V_{BR,}$ of the diodes between -7.8 V to -8.0 V at room temperature in the set of experimental diodes tested during last years. However, it is not in agreement with the ideal value that can be obtained for these epilayer properties, given for GaAs diodes from 100 to 500 K in [Schl01b] by,

$$V_{BR}(N_D,T) = (33.166 + 0.05224 \cdot T)\left(\frac{N_D}{10^{16}cm^{-3}}\right)^{-0.76} + 6.126 - 0.00333 \cdot T\,, \qquad (4.1)$$

where the predicted value of the breakdown voltage at N_D= $1\cdot10^{17}$cm^{-3} epilayer doping and room temperature T=300 K is V_{BR}= -13.61 V. Although it is not in agreement, we can use this equation to define an approximated value of a hypothetical new defined epilayer. A new epilayer doped at N_D= $2\cdot10^{17}$cm^{-3} has been proposed for the new 600 GHz doubler version, where the eq. 4.1 predicts a breakdown voltage 1.35 times smaller than at $1\cdot10^{17}$cm^{-3}. If we consider an equivalent tendency in the LPN PSBDs fabrication process, in accordance with the experimental results at $1\cdot10^{17}$cm^{-3}, the approximate value of the breakdown voltage for these new diodes at $2\cdot10^{17}$cm^{-3} would be around -5.9 V. A final breakdown voltage V_{BR}= -5.5 V has been proposed, being conservative, for this application at N_D= $2\cdot10^{17}$cm^{-3}.

Once the epilayer doping and the breakdown voltage are defined it is possible to define the epilayer thickness. The design of the doubler chip will be accomplished by considering that the excited voltage signal in the PSBDs does not exceed the breakdown voltage at any time. It means that the epilayer thickness is not bigger than the maximal depletion region depth during one period of the excited voltage signal in the PSBDs. The maximal depth of the depletion region can be calculated by eq. 2.4 at $V=V_{BR}$ = -5.5 V. In this case 210 nm of epilayer thickness of the PSBD is enough to contain the depletion region that will be generated in this application. I have initially considered a 250 nm epilayer thickness for the new PSBDs of the 600 GHz design in order to reduce a possible negative influence of the substrate on the PSBD RF performance.

It is finally necessary to define the anode size which is closely related with the expected input power managed by the PSBD. The considered full input power used for pumping this new doubler at 600 GHz is from 10 - 20 mW, in accordance with the experimental output power obtained in section 3.2 for the 300 GHz power-combined doubler. The input power for this module was ideally fixed at 15 mW. The anode size was found using ADS software in accordance with the available input power and the number of diodes in the doubler MMIC chip. Two MMIC chip with two and four anodes are compared in this section to choose the more suitable option for this application. It has been performed by defining a test-bench in ADS where the physical model SDD, developed during this doctoral work, is used for a single PSBD. It has been concluded that the second harmonic generation of a single PSBD and a pair of PSBDs in anti-series configuration are equivalent. Additionally, a 180 degrees phase shift would be required in the ADS test-bench between the excited LO signals in each diode to reproduce the anti-series configuration of the diode cell. Fortunately, it is possible to simplify the test-bench accounting for a single PSBD. The single PSBD is then connected to a one-tone source which generates the power and the frequency of the input LO power signal. Then, the different harmonics generated by the PSBD are separated using some filters in the ADS test-bench which allow us to optimize the impedance matching of the PSBD with the first and the second harmonic. The upper harmonics are connected to a 50 Ω load to emulate its mismatching in the real application. The results obtained with this procedure indicate the maximum ideal conversion efficiency and ideal matching impedance required by the first and second harmonics in the considered PSBD. However, it is necessary to choose the most suitable PSBD that maximizes the conversion efficiency in the full frequency band therefore, each considered anode size of the PSBD has to be tested in the full band with ADS and then compared between them to make a choice.

4.2.1.1 A Two-Anodes Chip Analysis

The analysis of the PSBD performance for a 600 GHz MMIC chip doubler when considering two anodes is carried out in this section. It is the starting point since we can compare the performance featured by the actual PSBDs used in section 4.1 and the new doubler. An 80-85 % of input signal coupling efficiency can usually be obtained with the PSBDs in this kind of device, thus an input power around 6-6.3 mW needs to be managed by each PSBD if 15 mW of input power is expected for pumping a two anodes doubler chip. This means that the PSBD anode size needs to be big enough to ensure that the optimal voltage

signal excited in the diode at any frequency of the band does not exceed the breakdown voltage of the epilayer. The physical properties of four different simulated PSBDs in the ADS test-bench using the developed SDD model are indicated in Table IV.1.

	Doping (cm^{-3})	W_{EP} (nm)	Area (μm^2)	R_S (Ω)	C_{j0} (fF)	V_{BR} (V)
D0	$1 \cdot 10^{17}$	350	3.5	26	4.4	-7.5
D1	$2 \cdot 10^{17}$	250	3.5	12.2	5.84	-5.5
D2	$2 \cdot 10^{17}$	250	4.49	9.8	7.54	-5.5
D3	$2 \cdot 10^{17}$	250	5.68	7.9	9.45	-5.5

Table IV.1. Physical and geometrical properties of the PSBDs considered in the two anodes 600 GHz doubler chip based on the design presented in section 4.1. The defined diode D0 is the same diodes used in the doubler presented in section 4.1 but the diodes D1, D2 and D3 are the new considered diodes in which the anode surface is swept, the epilayer doping has been doubled and the epilayer thickness reduced. A built-in voltage V_B= 0.75 V is considered in all cases.

Each diode presented in Table IV.1 has been individually simulated in the defined ADS test-bench, where the impedance matching of the first and second harmonic have been optimized for the optimal bias that ensures a voltage signal that does not exceed the breakdown voltage. The diode D0 is the current structure used in the 600 GHz doubler presented in section 4.1, the diode D1 is the same but with a change to the doping from $1 \cdot 10^{17}$ cm^{-3} to $2 \cdot 10^{17}$ cm^{-3} and a reduction in the epilayer thickness from 350 nm to 250 nm. The diodes D2 and D3 are a sweep of the anode size to compare with the D1 structure. The values of the series resistance emerge from the resistance SDD model developed during this doctoral work. It is important to state that the experimental rule $R_S \cdot C_{j0}$ depends on the epilayer doping and thickness. Additionally, this product slightly increases as the anode size increases. The comparison of the maximal second harmonic conversion efficiency of each single PSBD is plotted in Fig.

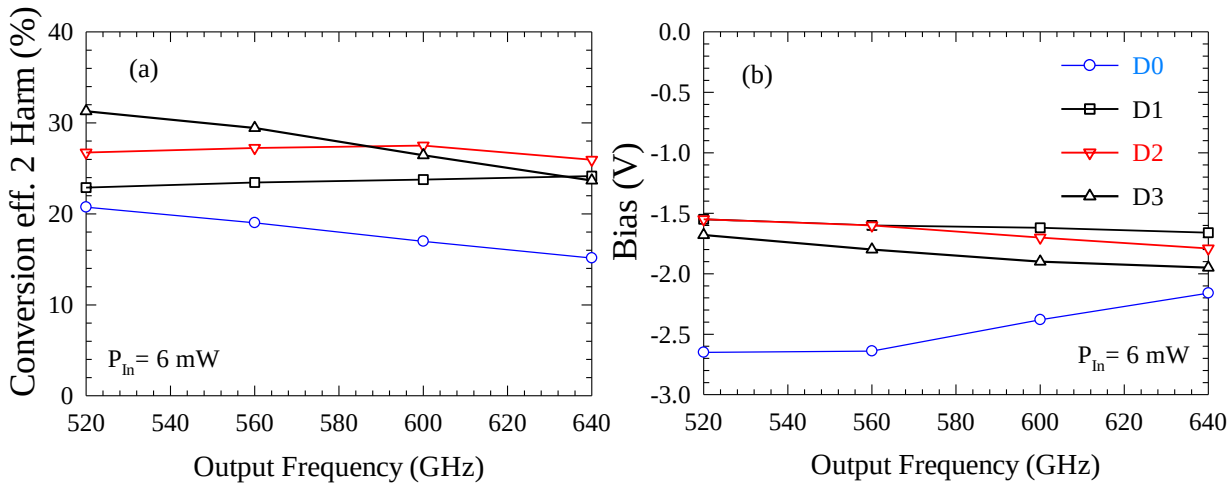

Fig. 4.12. (a) Conversion efficiency and the (b) bias obtained for the single analysis of the four different diodes presented in Table IV.1 when considering 6 mW of input power and the breakdown voltage specified. The legend affects both figures. Blue line corresponds to diode D0 and red line represents the preliminary option of the optimum case.

The diode D0, indicated in Fig. 4.11 in blue, represents the actual PSBD used in the doubler presented in section 4.1. These simulation results define the maximum second harmonic conversion efficiency of the PSBDs used in this chip when pumping it with 15 mW of input power. The simulation results of the second harmonic conversion efficiency presented in Fig.

4.11.(a) for diodes D1, D2 and D3 doped at $2 \cdot 10^{17}$ cm^{-3} of doping, show that the anode surface needs to be increased from 3.5 μm^2 (4.4 fF) to ≈4.5 μm^2 (7.6 fF) to obtain the best conversion efficiency in the full band, represented by diode D2 in red. A lower optimal reverse bias is required for the increased epilayer doping since the maximum depletion region is intrinsically reduced due to the additional charge. It has a very important consequence related to the presence of saturation phenomena. An increment of the epilayer doping together with the reduction of the optimal bias ensures the reduction of saturation phenomena when pumping these new PSBDs at ~300 GHz LO signal [Graj00b].

Once an approximation of the anode size is obtained, it is important to analyze the impedance matching of each simulated diode in order to determine the feasibility of the proposed two-anodes doubler chip. The real part of the first and second harmonic impedance optimization of each diode proposed in Table IV.1, are plotted in Fig. 4.13. We can see that the real impedance of the required new diode D2, for the first and the second harmonic, is almost half of the impedance required by the actual diode D0.

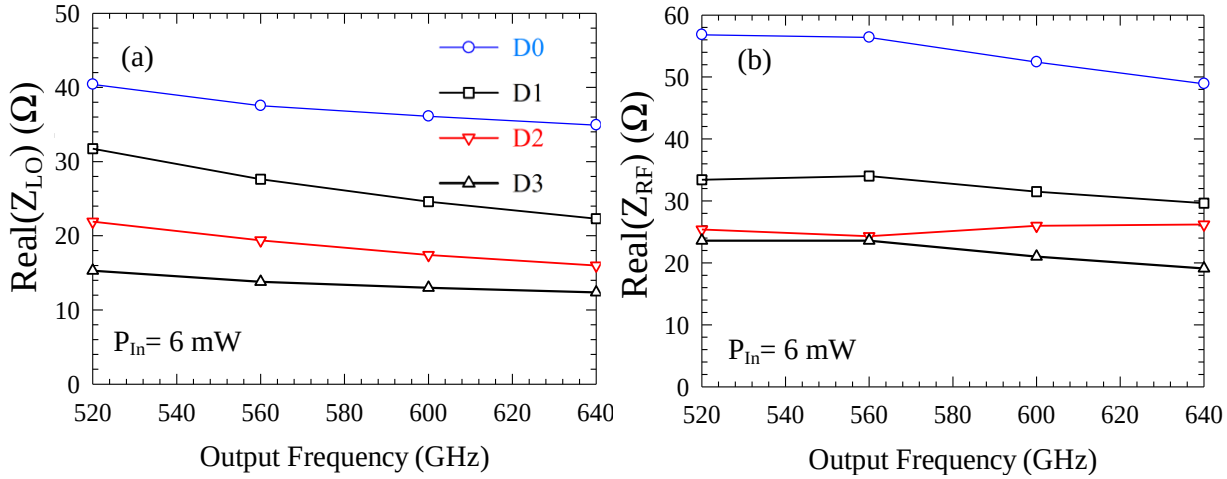

Fig. 4.13. (a) Real part of the first harmonic matching impedance and the (b) real part of the second harmonic matching impedance obtained from the single analysis of the four different diodes presented in Table IV.1 when considering 6 mW of input power per diode and the breakdown voltage specified. The legend affects both figures. Blue line corresponds to diode D0 and red line represents the preliminary option of the optimum case.

It is necessary to determine at this point if it is possible to define an impedance matching network, for the new PSBDs, consisting of the waveguides and transmission lines system. We first need to link the meaning of the results presented in Fig. 4.13, in terms of the doubler chip structure presented in Fig. 4.1. The input signal arrives at the chip and excites all diodes of the chip at the same time, since they are aligned with the electric field vector of the signal propagated by the waveguide in the TE_{10} mode. This means that the diodes present a kind of anti-series configuration for the LO input signal while they are in parallel configuration for the second harmonic, which is propagated in the chip in a quasi-TEM propagation mode of the transmission lines. Regarding the geometry of the input waveguide where the chip is inserted, an intrinsic impedance close to the diode cell impedance is required in order to be able to couple them. A 80-90 Ω intrinsic impedance waveguide section was necessary for the design of the 600 GHz doubler presented in Fig. 4.1, but a new 40-50 Ω impedance waveguide section would be necessary to match a two anodes chip based on the diode D2 of Table IV.1. Unfortunately, it is not feasible in practice because it requires a reduction of the

waveguide thickness while keeping the same height of the waveguide, which cannot be carried out in the mechanical block fabrication process. However, a higher intrinsic impedance waveguide section would be required if the diode cell consists of four anodes.

4.2.1.2 A four Anodes Chip Analysis

It was demonstrated in the previous section that more than two anodes doped at $2{\cdot}10^{17}$ cm^{-3} are required for this application between 540-640 GHz output frequency signal and 15 mW of available input power between 270-320 GHz. However, the anode size found in the previous section is not useful because half of power needs to be managed by each diode for a four-anodes doubler chip. The equivalent analysis presented in section 4.2.1.1 is repeated but considering 3 mW of input power to study the single diode response. The new set of simulated diodes using the developed SDD model is indicated in Table IV.2.

	Doping (cm^{-3})	W_{EP} (nm)	Area (μm^2)	R_S (Ω)	C_{j0} (fF)	V_{BR} (V)
D4	$2{\cdot}10^{17}$	250	2.74	15.2	4.71	-5.5
D5	$2{\cdot}10^{17}$	250	2.96	14.16	5.07	-5.5
D6	$2{\cdot}10^{17}$	250	3.24	13.1	5.53	-5.5
D7	$2{\cdot}10^{17}$	250	3.94	11.0	6.66	-5.5

Table IV.2. Physical and geometrical properties of the PSBDs considered in the four anodes 600 GHz doubler chip based on the design presented in section 4.1. A built-in voltage V_B= 0.75 V is considered in all cases.

Each diode presented in Table IV.1 has been individually simulated in the defined ADS test-bench, where the impedance matching of the first and second harmonic have been optimized for the optimal bias that ensures a voltage signal that does not exceed the breakdown voltage. The comparison of the resulting maximal second harmonic conversion efficiency of each single PSBD is plotted in Fig. 4.14.

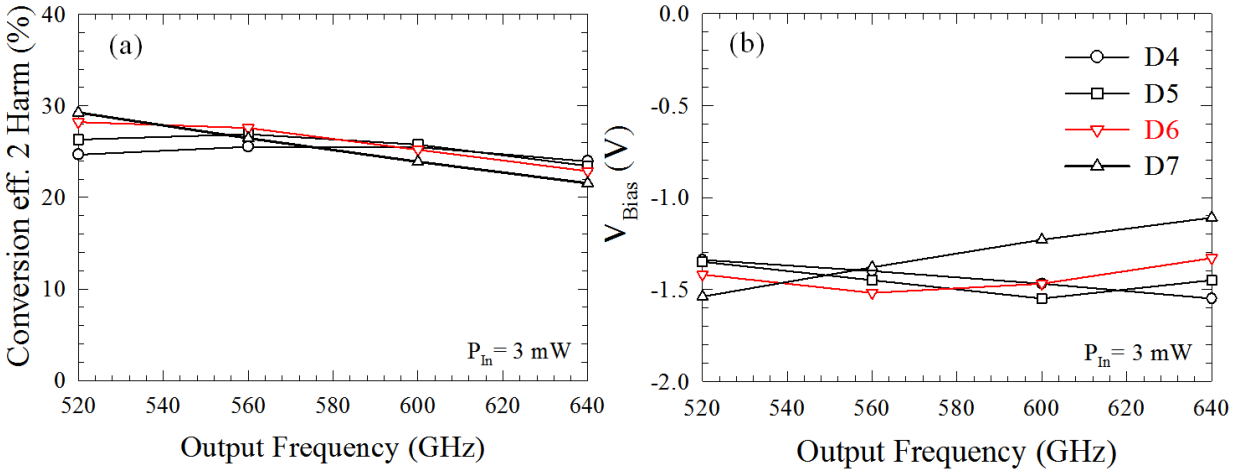

Fig. 4.14. (a) Conversion efficiency and the (b) bias obtained for the single analysis of the four different diodes presented in Table IV.2 when considering 3 mW of input power and the breakdown voltage specified. The legend affects both figures. The red line represents the closest option of the optimum case.

It is important to note in this second analysis that a small increment of the second harmonic conversion efficiency has been observed when comparing the results obtained if the minimum value of the excited voltage signal is limited to the breakdown voltage at -5.5 V or it is limited at -5 V or even -4.5 V. For this reason the minimum value of the excited voltage signal has

been reduced to -4.5 V, which allows keeping the results obtained in Fig. 4.12 while it opens the possibility to reduce the epilayer thickness from 250 nm to 200 nm without degrading the capacitance behavior. It can be observed in Fig. 4.14 that the maximum efficiency remains at similar values previously obtained in Fig. 4.12, but the anode size of the most suitable diode returns to similar values used for the doubler presented in section 4.1. Although the anode size proposed for the redesign 600 GHz doubler chip at 4 anodes is very similar to the anode size of the first version at two anodes, each new PSBD is expected to manage half of input power while featuring half of series resistance (~13 Ω) and a slightly higher capacitance (C_{j0}~5.5 fF). These results indicate that the new PSBDs proposed for the redesigned 600 GHz chip should dissipate the unconverted input power in a bigger distributed area of the chip and it should be less affected by self-heating phenomena. Additionally, no remarkable saturation phenomena are expected in these new PSBDs in accordance with [Graj00b], previously mentioned in section 4.2.1.1. However, it is necessary to check the impedance matching feasibility according to the impedance of the proposed diodes.

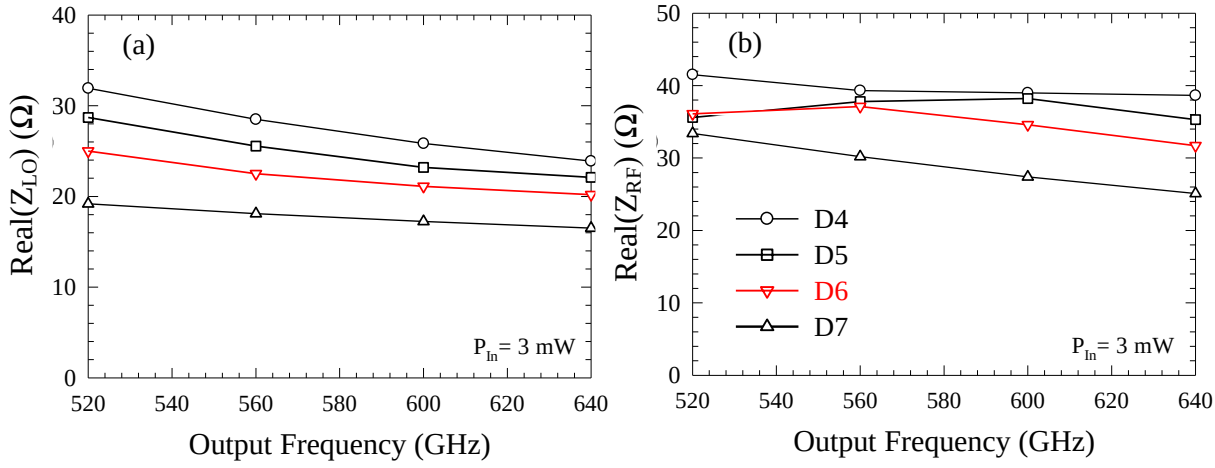

Fig. 4.15. (a) Real part of the first harmonic impedance and the (b) real part of the second harmonic impedance obtained from the single analysis of the four different diodes presented in Table IV.2 when considering 3 mW of input power and the breakdown voltage specified. The legend affects both figures. The red line represents the closest option of the optimum case.

We can see in Fig. 4.15.(a) that the real part of the first harmonic of the PSBD D6 is around 22-24 Ω, which is slightly higher than the impedance obtained in diode D2. However, this PSBD is proposed for a four-anodes 600 GHz doubler chip where the required intrinsic waveguide impedance would be between 90-110 Ω, which is some ohms higher than the design presented in section 4.1. This means that the MMIC chip and the input waveguide would be wider, which simplifies the mechanical block fabrication process. However, it is necessary to thoroughly analyze the interaction between the propagation modes generated by the chip and the input waveguide section. A wider input waveguide could couple the TM_{11} mode of the second harmonic generated by the diode cell.

We conclude this section with the analysis of the mentioned reduction of the epilayer thickness. The predicted second harmonic conversion efficiency given by diode D2 in Fig. 4.12 presents a conversion efficiency around 24-25 % in the considered band when limiting the exited voltage signal at -5.5 V. The diode D6 in Fig. 4.15 presents a conversion efficiency around 22-24 Ω in the same band when limiting the excited voltage signal at -4.5 V. This

indicates that most of the conversion efficiency comes from less reversed biased regions of the C-V characteristic. Additionally, better maximal conversion efficiencies are systematically predicted by the developed SDD model when reducing the input power to be managed by an optimized PSBD. Unfortunately, several versions of the same application optimized at different input available powers would be required to experimentally demonstrate this observation. The interest in optimizing the new 600 GHz doubler with a minimum excited voltage signal value at -4.5 V is the possibility of reducing the thickness of the epilayer. This does not negatively affect the varactor mode of the PSBD but it reduces the series resistance of the diode. Using the analytical equation of the depletion region depth given by eq. 2.4 at -4.5 V, we obtain a ~190 nm depletion region depth. It allows redefining the epilayer thickness at 200 nm. The comparison of the results obtained for diode D6 when considering a 250 nm and a 200 nm epilayer thickness is presented in Fig. 4.16.

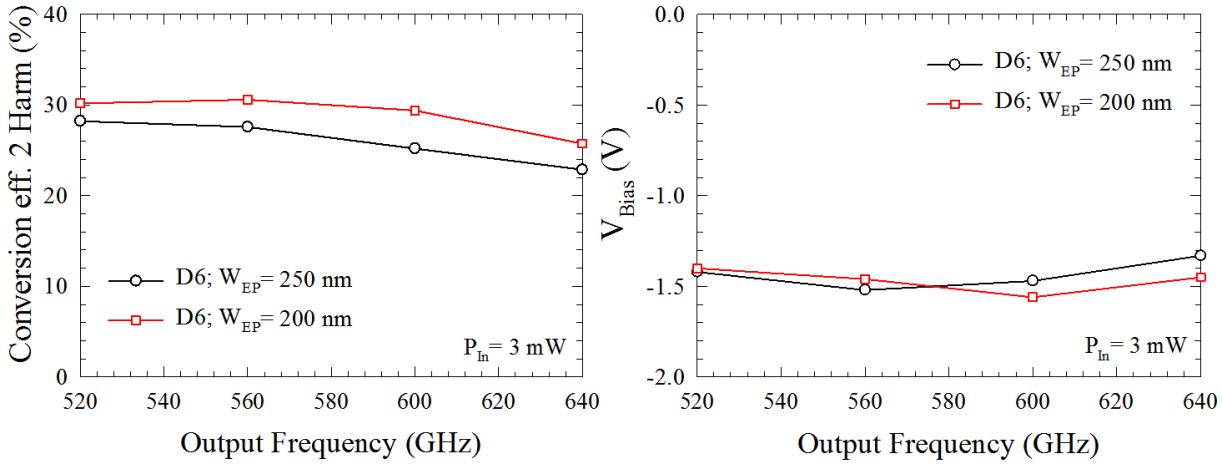

Fig. 4.16. (a) Conversion efficiency and the (b) bias comparison obtained for the single analysis of the diode D6 presented in Table IV.2 when considering an epilayer thickness of 250 nm and 200 nm. A 3 mW of input power is used to pump the diode.

We can see an increment of the second harmonic conversion efficiency in the band around 2-3 % compared with the case at 250 nm epilayer thickness and a reduced series resistance R_S= 11.2 Ω. The important point is that the optimal bias is very close in both cases since they have an equivalent C-V characteristic. However, we have to analyze the impedance in both cases in order to conclude if there would be an equivalent LO and RF coupling. The impedance of the first and second harmonic in diode D6 at 250 nm and 200 nm epilayer thicknesses are plotted in Fig. 4.17. The similarity of the impedances in both cases indicates a correct coupling in the proximities of the ideal bias. We conclude this section with a selected PSBD for the redesigned 600 GHz chip. It features four anodes with ~3.25 μm^2 surface and a 200 nm epilayer thickness doped at $2 \cdot 10^{17}$ cm^{-3} that have been optimized to manage 3 mW of input power between 270-320 GHz. This results in a junction capacitance C_{j0}= 5.5 fF and a series resistance R_S= 11.2 Ω. It has been optimized for a voltage signal that does not exceed -4.5 V, which is at ~1 V from the expected breakdown voltage. These decisions lead to a redesigned chip where each diode manages half of the power managed by the PSBDs used in the 600 GHz two-anodes doubler presented in section 4.1 while the surface of these redesigned diodes is similar.

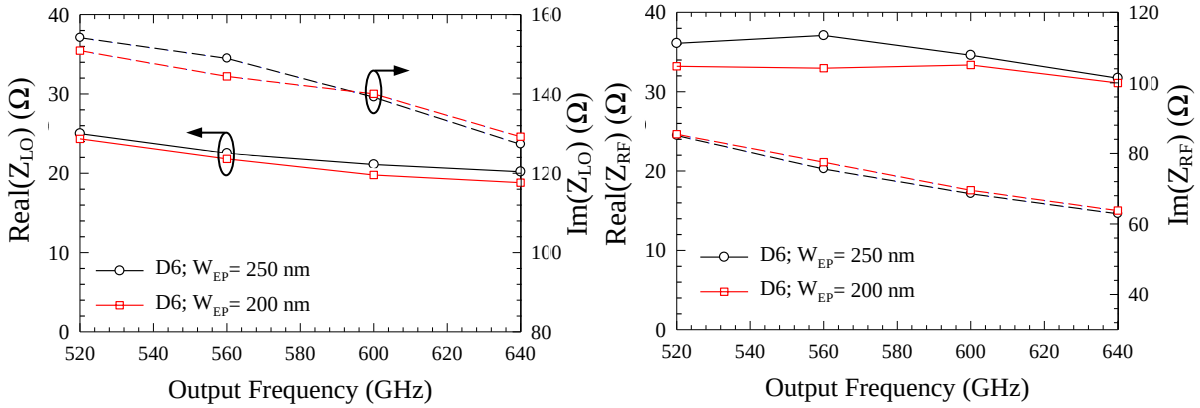

Fig. 4.17. (a) First harmonic and the (b) second harmonic real (solid lines) and imaginary (dashed lines) impedances obtained for the single analysis of the diode D6 presented in Table IV.2 when considering an epilayer thickness of 250 nm and 200 nm. A 3 mW of input power is used to pump the diode.

A lower influence of self-heating phenomena is expected in this new design. The new PSBDs have been optimized for an excited voltage signal far from the breakdown voltage. Therefore, no additional second harmonic generation phenomena are expected from the breakdown current. In addition, reduced saturation phenomena are expected due to the increment of the doping level and the reduction of the optimal bias of each PSBD. It is important to remark that this redesign of the PSBDs has been purely accomplished in terms of the developed SDD model. Thus we have been very conservative in many assumptions that need to be experimentally verified. Further improvements for this application can probably be accomplished in the future based on experimental results of the proposed design.

4.2.2 Virtual Design in ADS-HFSS

Once the PSBDs are defined for the application, it is possible to start the design of the MMIC chip and the matching network which allows obtaining the best possible performances. The final HFSS design of the 600 GHz four anodes chip is first present in Fig. 4.18, and the analysis of each stage of the development is then discussed along this sections. The MMIC chip features an anti-series set of four planar Schottky diodes integrated within the suspended microstrip circuit on a 4 μm-thick GaAs membrane placed in a split mechanical block by metallic beam-leads. The diodes are in a balance configuration in a way that the odd harmonics are generated in opposite phase by each branch of the diode cell while the even harmonics are generated in phase. It results in odd harmonics annihilation leading to a more simple and compact design where only even harmonics are propagated in the chip. The input LO signal reaches the MMIC chip led by waveguides in which the height (864 μm) is specifically designed to transmit the TE_{10} mode at the input frequency signal range and cut off the TM_{11} mode. The input structure of the device is designed for coupling the diode cell with the TE_{10} mode, transmitted in the input waveguide, where the generated odd harmonic are eliminated while the even harmonics are propagated in a quasi TEM transmission line mode to the output stage of the MMIC chip by an intermediate channel which separates the input and output waveguides. The thickness of the input waveguide section that reaches the chip is designed to match the diode cell LO impedance and cut off the upper propagation modes that could be coupled with the generated second harmonic by the diode cell. A high-low

transmission hammer filter optimized for cutting off the second harmonic is used to avoid losses of the desired signal in the DC circuit which is connected to a SMA connector in the mounted device.

The 600 GHz doubler chip was optimized for 3.0 mW of LO power per diode, i.e., the full chip is optimized for ~15 mW of LO input power between 260 – 320 GHz if around 80-85 % of LO coupling efficiency is considered. The epilayer is doped at $2 \cdot 10^{17}$ cm^{-3} and it features a 200 nm thickness. The nominal anode size of each diode is ~3.25 μm^2, which results in a junction capacity $C_{j0} \approx 5.5$ fF (using eq. 2.21). The anode size results of the considered nominal power (~3.0 mW in this case), the epilayer doping level, the epilayer thickness and the frequency range. A 11.2 Ω series resistance was considered in the development of this device, in accordance with the study developed in section 4.2.1 and the experimental results obtained with the 600 GHz two anodes doubler. The final diode properties and the number of diodes considered in the chip will define the geometry of the input section of the waveguides/transmission lines. The length of the middle channel and the output waveguides geometry results of an optimal coupling between the generated second harmonic in the diode cell and the output antenna.

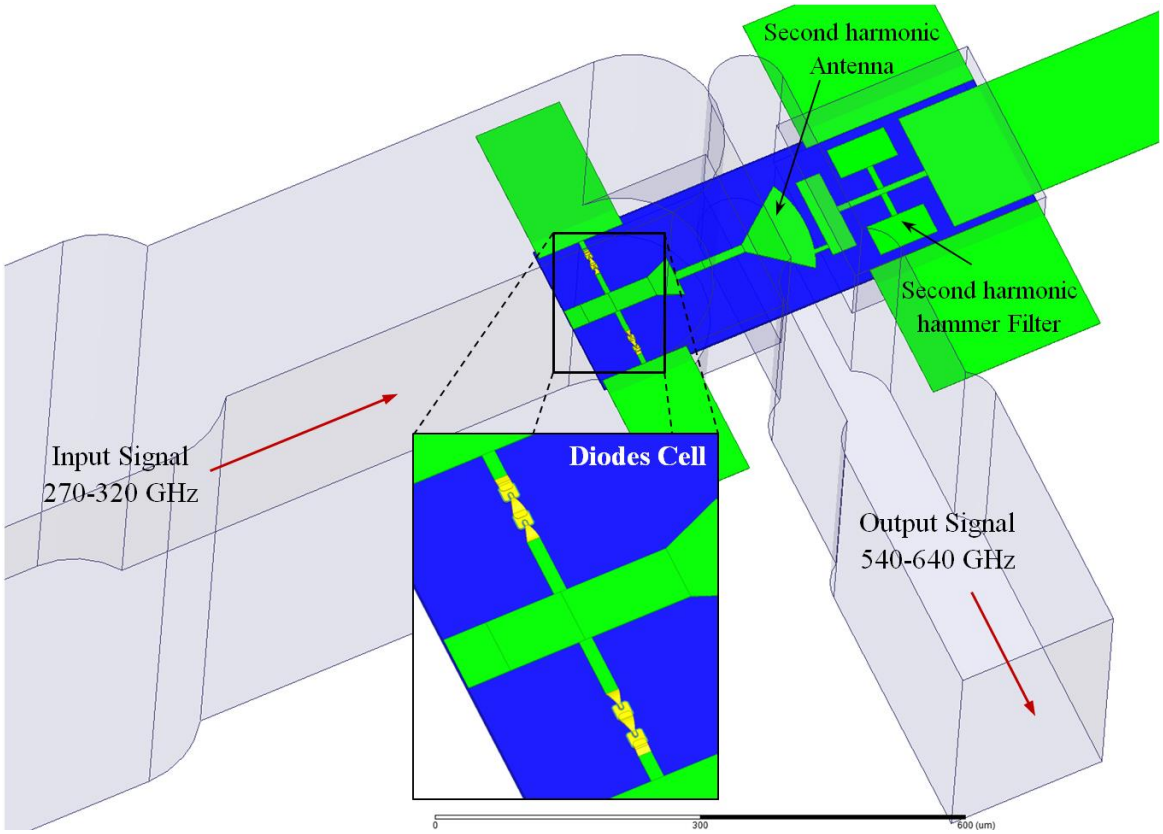

Fig. 4.18. LERMA HFSS 3D design of the 600 GHz four anodes frequency doubler where the different parts of the MMIC chip are indicated. The balance configuration of Schottky diodes is specifically noted. A hammer filter is used to block the second harmonic signal to come out of the chip by the DC circuit.

4.2.2.1 Input Stage Design

The input stage of the chip is the most critical point and needs to be clearly defined at the beginning of the design. It is necessary to find the width of the input waveguide that arrives into the chip and can match the input signal with the diode cell impedance. However, it is

necessary to ensure that the width of the input waveguide that correctly matches the input signal with the diode cell does not match the generated second harmonic with some upper propagation modes of the input waveguide.

A. The Diode Cell

The width of the waveguide has to be large enough to place the set of diodes and the ratio height-width has to be technically feasible in practice. We have mentioned in section 4.2.1 that the intrinsic impedance of the input waveguide section needs to be similar to the addition of the first harmonic real impedances of the four PSBDs (90-110 Ω) placed in an anti-series configuration with respect the electric field vector of the TE_{10} propagation mode of the waveguide. The first point is to simulate the diode cell section in HFSS. We define one port for each diode and select an integration line parallel to the electric field vector and in the same direction, as illustrated in Fig. 4.19 by HFSS simulations of the diode structure. In Fig. 4.19.(a) the PSBDs are shown simulated in HFSS where the Schottky anode, the ohmic contact and the GaAs mesas are indicated.

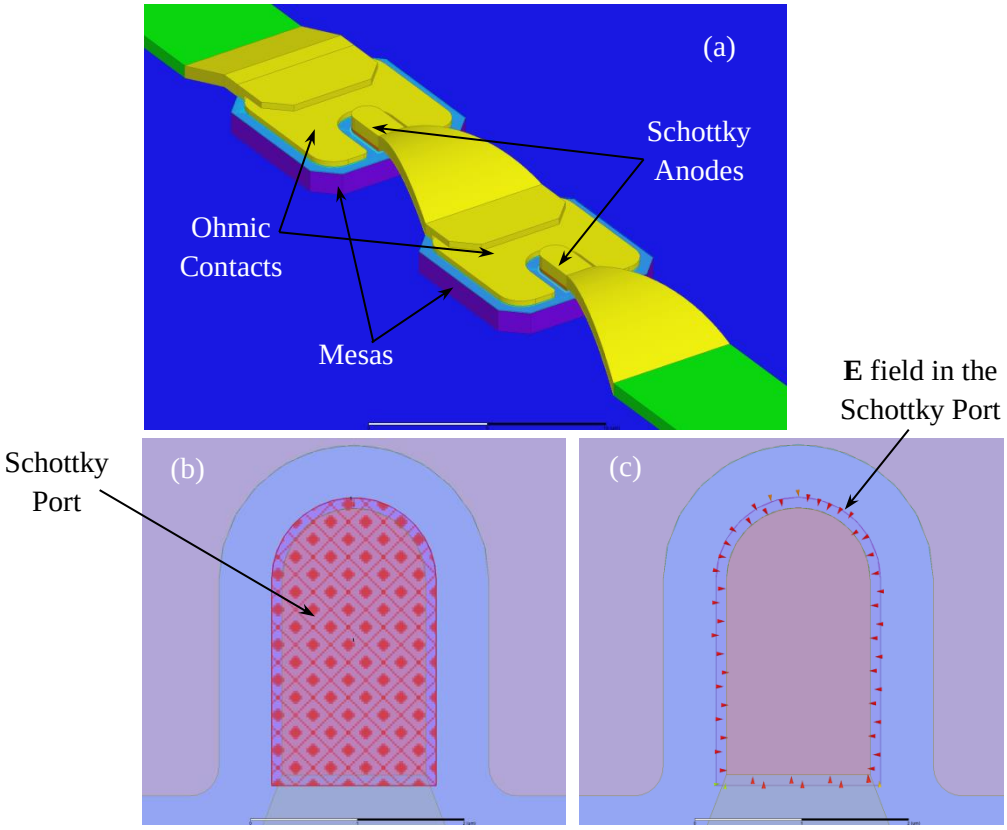

Fig. 4.19. HFSS 3D design of the (a) PSBDs defined in the 600 GHz four anodes frequency doubler where the different parts of the diode are indicated. The (b) defined port and the (c) electric field vector in HFSS simulations have been indicated to illustrate the diodes definition.

These PSBDs' structures are presented in [Maes10]. The light blue layer is the dielectric used in the passivation of the epilayer. The defined port of the Schottky contact is shown in Fig. 4.19.(b) where it is possible to appreciate that it has exactly the same profile as the Schottky anode but is slightly larger and it is defined in a surface under the metal of the anode. The resulting electric field vector simulated in HFSS is plotted in Fig. 4.19.(c) where the electric field direction heads towards the metal of the anode and it is limited to the space

between the profile of the defined port and the metallic anode, representing a kind of coaxial line. The difference between the surface of the port and the anode has to be small enough to correctly simulate the parasitic impendences between the Schottky anode, the ohmic contact, the air-bridge and the mesa.

B. LO signal modes

We can simulate the ensemble of PSBDs in the diode cell of the chip by considering the geometry of the section which contains the diode in Fig. 4.18. This section consists of a waveguide (section 864x210 μm^2) in which the diodo cell of the MMIC chip has been placed in parallel with the electric field vector of the TE_{10} input signal propagation mode of the waveguide and centered in the middle of the waveguide where the electric field reaches the highest intensity. The excited signal in the diode cell, containing only the even harmonics, is then propagated in the chip in a quasi-TEM mode of the transmission lines. There are only two propagation modes to be simulated for the input signal between 270-320 GHz, the TE_{10} mode of the waveguide and the quasi-TEM mode of the transmission line, which are plotted in Fig. 4.20. All upper modes of the waveguide are cut off in the frequency range of the LO signal and there is only one possible quasi-TEM mode. The TE_{10} mode of the waveguide presents an electric field vector perpendicular to the pointing vector. The quasi-TEM mode presents a radial configuration of the electric field lines, and it is excited in the diode cell due to the parallel configuration of the PSBDs with respect to the electric field vector of the waveguide TE_{10} mode. The intrinsic impedance of the waveguide section (864x210 μm^2), which contains the diode cell, has been simulated in HFSS and it has a Z_0= 113 Ω.

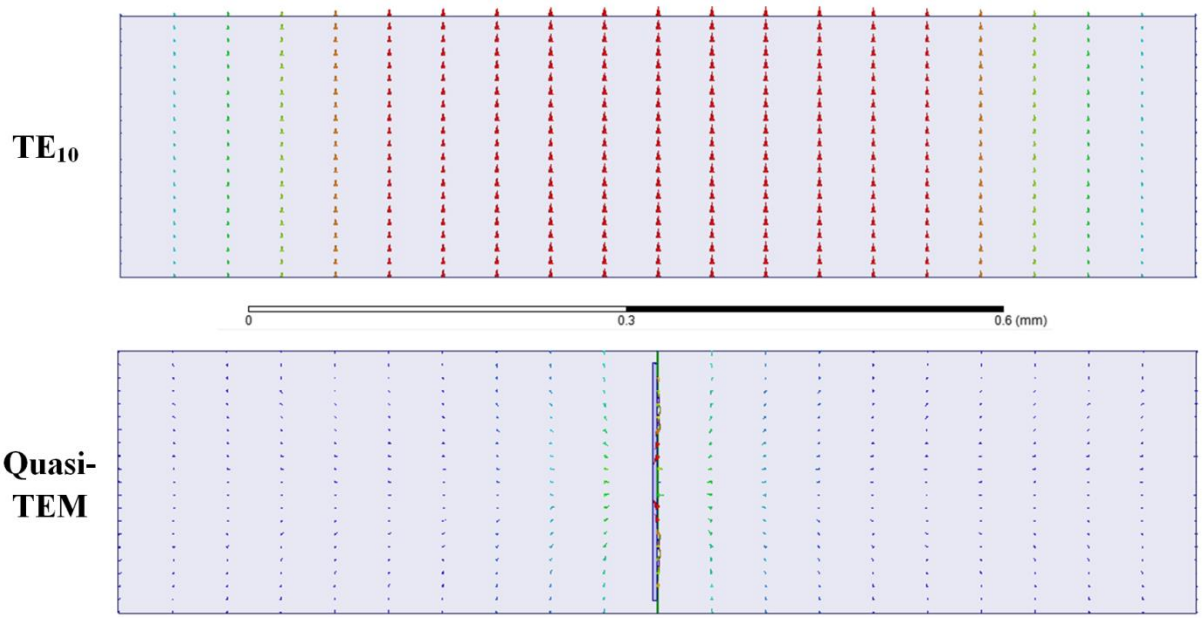

Fig. 4.20. TE_{10} propagation mode in the waveguide and the quasi-TEM propagation mode in the transmission line in the proximities of the diode cell, simulated in HFSS at 320 GHz. No additional propagation modes can be transmitted.

The intrinsic impedance of this section of the chip is similar to the addition of the real impedance of the PSBDs, as previously discussed. This impedance is mainly defined by the waveguide thickness where the chip is placed. However, the final optimal structure depends on the GaAs membrane thickness, the width of the central transmission line and the

transmission lines which connect the PSBDs. The input power arrives at the diodes in a TE_{10} mode which excites the same signal in both PSBD branches of the chip but 180 degrees shifted in phase due to the anti-series configuration. This shift in the excited signal in the PSBDs by the input signal, results in an opposite phase generation of the odd harmonics while the even harmonics remain in phase. Once the input power is coupled with the diode cell, the odd harmonics annihilate themselves in the center of the diode cell and only the even harmonics of each branch are added and transmitted in the central transmission line in a radial quasi-TEM mode.

C. RF signal modes

The analysis of the propagation modes that can exist in the device for the second harmonic, generated by the PSBDs, is a very critical point to ensure an acceptable design of the device.

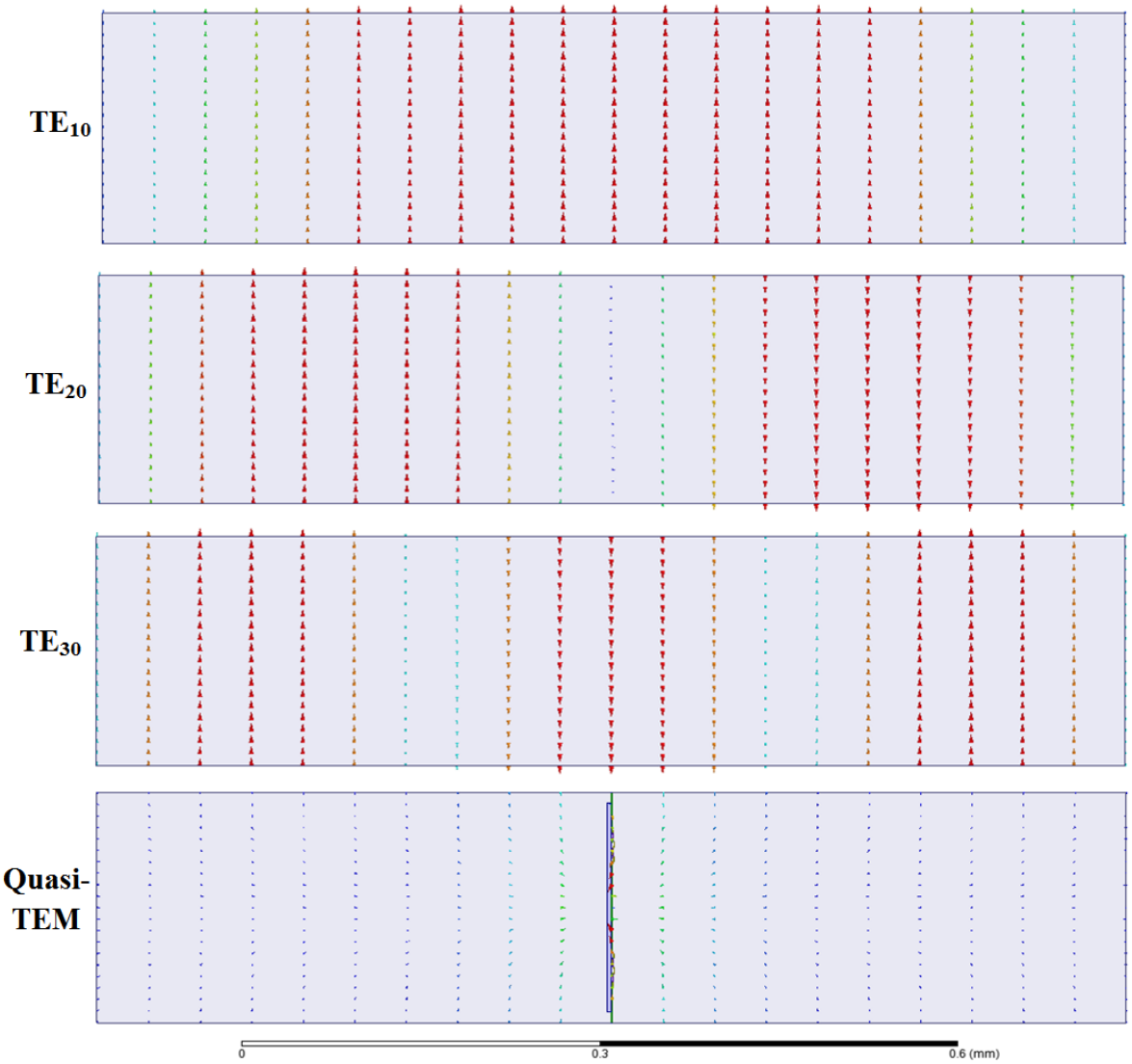

Fig. 4.21. TE_{10}, TE_{20}, TE_{30} propagation mode in the waveguide and the quasi-TEM propagation mode in the transmission line, simulated in HFSS at 640 GHz. No additional propagation modes can be transmitted.

Additional propagation modes of the input waveguide appear for the second harmonic and it is necessary to ensure that these upper propagation modes are not coupled with the generated signal in order to avoid losses. The new propagation modes that can exist in the input

waveguide (section 864x210 μm^2) at 640 GHz have been plotted in Fig. 4.21. The waveguide propagation modes that can be transmitted in the input waveguide are the TE_{10}, TE_{20} and TE_{30} modes. The quasi-TEM mode associated with the transmission line remains the only one since it depends on the number of metallic lines instead of the frequency. The TE_{20} mode is not a problem since its electric field lines pattern is not suitable to be coupled with the TEM mode generated by the PSBDs. However, the TE_{30} and especially the TE_{10}, present a similar electric field pattern in the middle of the waveguide and they can potentially be coupled with the radial quasi-TEM mode. The coupling of the RF quasi-TEM mode with the TE_{10} and TE_{30} modes of the input waveguide is avoided due to the balance configuration of the PSBDs. The second harmonic signals generated by each branch are transmitted radially and in phase toward the center of the diode cell where they are coupled with the central transmission line quasi-TEM mode. The radial transmission of the second harmonic in the diode cell is not compatible with the TE_{10} and TE_{30} waveguide modes, while it correctly fits the radial distribution of the electric field vector in the quasi-TEM mode that can be propagated in the central transmission line. It finally results in a quasi-TEM mode which is the easiest propagation mode to be coupled by the diode cell in the second harmonic frequency range.

It is possible to conclude that the design presented in Fig. 4.18, does not have leaks of the second harmonic into the input waveguide and it has enough room to seat the four PSBDs. We can also comment that it would not be possible to redesign a 600 GHz six anodes doubler chip using the same PSBDs to increase the handled power (3 mW per diode) because it would require increasing the input waveguide section. It has been determined during this study that a 864x250 μm^2 waveguide section allows the propagation of the TM_{11} mode at 640 GHz. This mode has been simulated and plotted in Fig. 4.22, where it is possible to remark the equivalent radial distribution of the electric field lines in the TM_{11} mode and the quasi-TEM mode of the central transmission line.

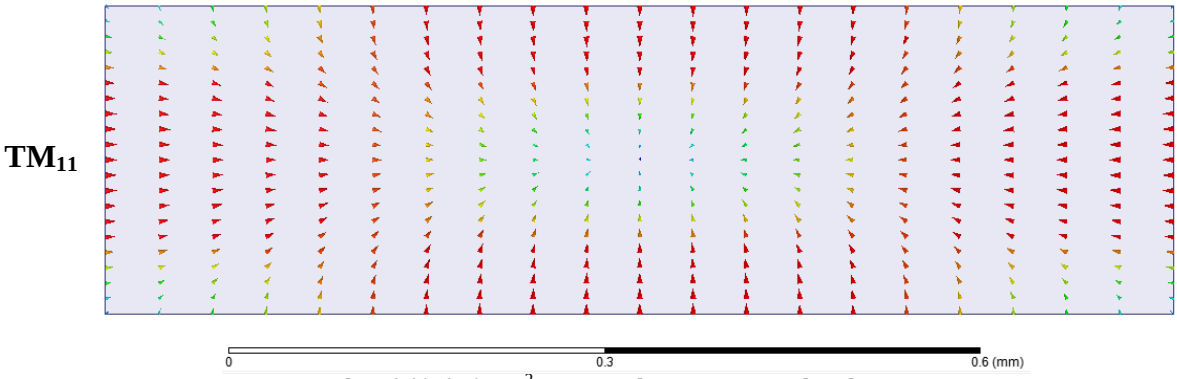

Fig. 4.22. TM_{11} propagation mode a 864x250 μm^2 waveguide section, simulated in HFSS at 640 GHz.

If the TM_{11} mode can be propagated in the input waveguide, a part of the generated second harmonic signal would be coupled and lost in the input waveguide.

4.2.2.2 LO and RF Coupling Optimization

The relationship between the dimensions and geometry of the chip with the input and output frequency signals is analyzed in this section. The waveguide matching network of the new 600 GHz doubler design is shown in Fig. 4.23.

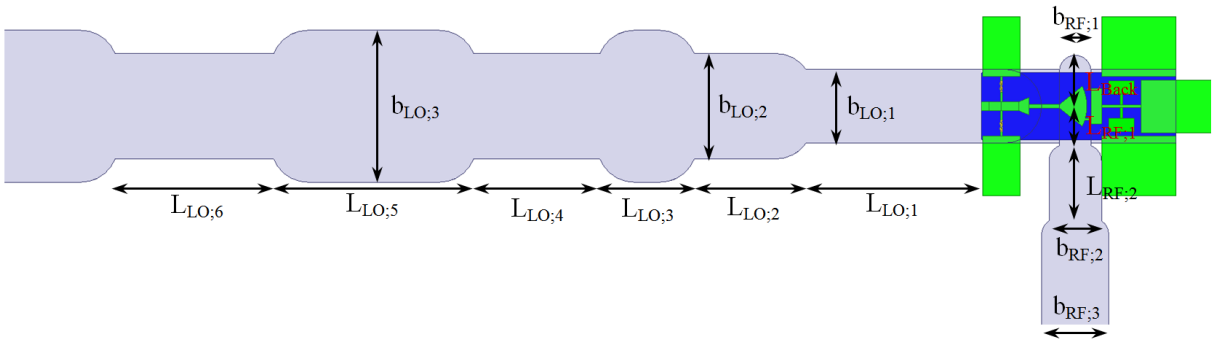

Fig. 4.23. Final design of the LERMA 600 GHz four anodes doubler chip and the waveguides matching network simulated with ADS-HFSS softwavers.

It is possible to observe 15 different dimension parameters indicated in Fig. 4.23 and there are 20 additional parameters to be defined in the 600 GHz four anodes doubler chip in Fig. 4.24 where the final HFSS design of the chip has been shown. There are more than 35 parameters to optimize in this system which are non-linearly related. The optimization process we have discussed in chapter 1 becomes the main tool we have at this point to face this complex system. A qualitative comprehension of all these parameters is discussed in this section.

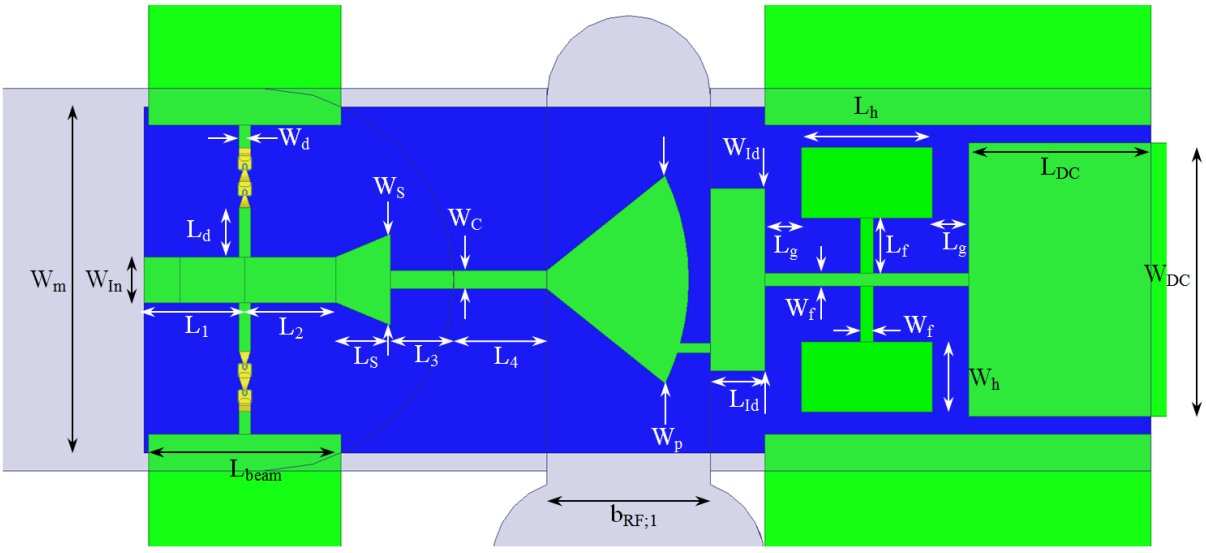

Fig. 4.24. Final design of the LERMA 600 GHz four anodes doubler chip simulated with ADS-HFSS softwavers.

A. Second harmonic antenna and hammer filter

We can start discussing the output stage of the chip, but it is designed after the input stage. It first consists of a L_4 middle channel length where the dimensions of the waveguide are chosen to fit the input waveguide width and its height is reduced to avoid any propagation mode except the TEM propagation mode of the transmission line. Second, it features the second harmonic antenna followed by the second harmonic hammer filter.

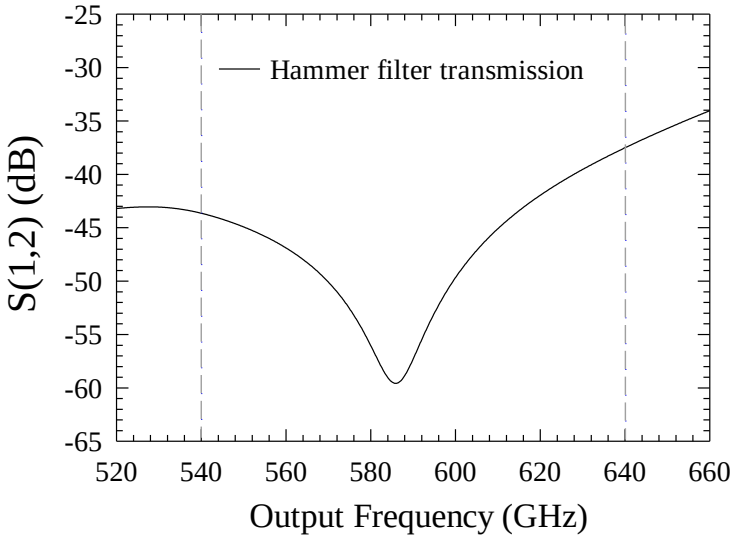

Fig. 4.25. Transmission of the second harmonic in the hammer filter used in the 600 GHz four anode chip design presented in Fig. 4.24.

The hammer filter is the first optimization to be performed, where the dimensions W_f, L_g, W_{DC}, L_{DC} and W_{Id} can be fixed in accordance with the general dimensions of the chip and a very basic version of the antenna and the output waveguides can be considered. Then, the L_h, W_h and L_{Id} parameters can be optimized to minimize the S-parameter S(1,2) or maximize S(1,1), where 1 represents the input side of the second harmonic signal into filter and 2 represents the other side, where the DC circuit is connected with. A preliminary optimization of the second harmonic antenna can then be carried out by optimizing W_p and $L_{RF;1}$ with the previously optimized hammer filter. After some optimization work with this preliminary output stage design together with the previous input stage it is possible obtain an approximation of the final output matching network of waveguides. A final optimization of W_p and $L_{RF;1}$ can be accomplished to obtain the final output stage design. The S(1,2) parameter represented in Fig. 4.25, corresponds to the power transmission of the second harmonic from the middle channel to the DC circuit in the final 600 GHz four anodes doubler. It is lower than -40 dB in most of the band and less than -50 dB in the center of the band. The performance of this hammer filter is better than in the 600 GHz two anodes doubler because the chip is wider, allowing a better optimization.

B. LO and RF diode cell coupling

This is the most critical part of the design because the geometrical parameters that control the RF coupling are completely linked with the LO coupling of the PSBDs. These kinds of doublers have demonstrated to couple up to 75-90 % of the input power into the PSBDs in broadband devices. The LO coupling of the diodes is obtained by generating a standing wave that oscillates in the proximities of the diodes at the LO frequency. This means that L_1, L_2, L_S and L_3 define half of the total path followed by the LO signal, between the reflected and the incoming signal which generate the standing wave that couples the diodes. However, this approach to couple the input power with the diode cell makes these devices sensitive to additional standing waves. The standing waves are generated in the waveguide system between the different stages of the multiplication chain, which oscillates with a different frequency and modifies the position and impedance of the optimized standing wave signal.

The impedance of the waveguide section, where the standing wave is coupled with the diode cell, can be controlled by optimizing the length parameters $L_{LO;i}$. The width of the cavities defined in the input waveguide system by $b_{LO;2}$ and $b_{LO;3}$ can be fixed in order to define an impedance step between sections. The parameter $b_{LO;1}$ is fixed in accordance with the adequate value discussed in section 4.2.2.1. The cavities defined in the input waveguide system allow controlling the impedance dependency on frequency of the standing wave which couples the diode cell thereby allowing a wideband LO coupling. Equivalently, the parameters $b_{RF;i}$ and $L_{RF;i}$ defined in the output waveguide system are optimized to fit the impedance dependence on frequency of the antenna to correctly extract the second harmonic from the chip.

However, the geometrical parameters W_m, W_{In}, L_1, L_2, L_S, W_S, W_C, L_d, W_d and L_3 are dedicated to the second harmonic matching. This means that we have to find the set of parameters that couple the generated second harmonic by the PSBDs while the LO input power is still coupled with the diode cell. We can now summarize some of the linked geometrical parameters:

1- The length parameter L_1 is always the same independently of all the others geometrical parameters. This dimension is completely related to the center frequency of the second harmonic range and the electrical path followed by the second harmonic generated in the PSBDs, i.e., the L_1 length is used to reflect the second harmonic generated by the diode cell and its value has to be the smallest one that ensures a constructive interference between the second harmonic signal reflected at the edge of the chip and the generated by the diode cell in any instant. The value of L_1 is always around a multiple of $\lambda/4$, where λ is the wavelength of the central frequency of the considered frequency band. We have to note that a signal transmitted in a transmission line TEM mode finishes a period in $\lambda/2$.

2- The objective is to reduce the self-heating effects that could degrade the PSBDs and we can do this by defining the dimension W_d as wider as possible. The W_d parameter is closely related with L_d, the GaAs membrane thickness and the central transmission line width W_{In}. If we fix the value of W_d, there are numerous sets of values for the rest of parameters that will get a second harmonic well matched but only a few set of values that will also keep the LO input signal matched. The relationship between the input waveguide width $b_{LO;1}$ and the transmission line length L_2, is very important at this point. The wider the input waveguide is, the shorter the L_2 parameter necessary to correctly match the second harmonic. This means that the input waveguide width $b_{LO;1}$ has the main role in the relationship that allows optimizing the LO and RF coupling, especially led by the parameters L_2, L_S and L_3.

3- The dimensions L_S and W_S of the impedance step can be related to the central transmission line geometry. The parameter W_S is usually two times wider than the W_{In} line and the parameter L_S can by fixed between the W_S and the L_S value. This step is used to introduce a smooth impedance step between the second harmonic generated by the diode cell and the output line through the middle channel, while this impedance step is higher in the opposite sense. It helps to isolate the diode cell and the reflected second harmonic signal in the step between the input waveguide height and the narrow middle

channel. This finally results in minimum L_3 parameter length that stabilizes the interaction between the middle channel and the RF matching of the diode cell.

4- The width of the central transmission line W_{In} is very dependent on the defined input waveguide width $b_{LO;1}$. If we have a good RF matching but a bad LO matching it is necessary to modify $b_{LO;1}$. If $b_{LO;1}$ is increased, the intrinsic impedance of the input waveguide increases, and it requires a modification of W_{In} in order to recover the RF matching. W_{In} would need to be increased, if $b_{LO;1}$ is increased, to reduce the incremented impedance of the transmission line introduced by $b_{LO;1}$,. The pair of diodes in each branch of the diode cell are defined as close as possible in the design presented in Fig. 4.24 and their position is controlled by L_d. It is a very important parameter when $b_{LO;1}$ and W_{In} are already stablished because L_d allows to modify the RF matching along the frequency band. It allows the recalibration of the global performance of the device in accordance with the LO coupling, favoring the second harmonic generation in the most critical frequencies. That is to say, it allows promoting the high/low frequencies RF matching if there is an unexpected LO mismatching at high/low frequencies.

5- The dimensions L_2 and L_4 are closely linked for the second harmonic coupling between the diode cell and the RF antenna. The shorter the L_2 length is, the larger the L_4 parameter necessary to correctly match the RF antenna with the middle channel signal. It is because the TEM mode in the middle channel has to reach the antenna in an optimal phase that is especially controlled by L_2 and L_4 to keep a similar electrical path between the diode cell and the antenna, which is around multiples of $\lambda/2$. It is possible to have a relationship between $b_{LO;1}$, W_{In} and L_2 that leads to a too small optimal value of L_4 to couple the RF antenna during the design, which is not feasible in practice. In this case, it is necessary to increase L_4 to find the next multiple of $\lambda/2$ that will allow matching the second harmonic generated by the diodes and the RF antenna. It is probably the case obtained at JPL in the design of 200, 400 and 800 GHz doublers [Schl01a], [Schl01b], [Schl02], where the "substrateless" concept is implemented to reduce the transmission losses in such a long middle channel.

In conclusion, the discussion presented in this section describes the main role of the different structures and geometries of the MMIC chip presented in Fig. 4.23. The most critical point is the PSBDs properties that define the required number of diodes to be included in the design. In addition, a thorough analysis of the diodes properties, presented in section 4.2.1, is vital when completely changing the PSBDs characteristics. The main geometrical parameter that defines the feasibility of a design with such diodes properties is the input waveguide width $b_{LO;1}$. On one hand, if the required $b_{LO;1}$ width to match the diode cell is too wide, the TM_{11} mode would be coupled and a part of the second harmonic generated by the diodes would be lost in the input waveguide system. On the other hand, if the required $b_{LO;1}$ width is too small, the fabrication of such a thin and deep input waveguide is not feasible due to the milling drum standards used to fabricate the mechanical block. If the required $b_{LO;1}$ value to match the LO signal with diodes is within the feasible range, a set of parameters always exist that can match the RF signal generated by the diodes. The RF antenna and filter system is the last point to be accounted for and it defines the efficiency of the chip to couple the second

harmonic generated by the diodes with the output waveguide system. The design of the output stage can be determined by the considered bias system.

4.2.3 Virtual ADS-HFSS Comparison between the 600 GHz two and four Anodes Doublers

The simulation results obtained in ADS-HFSS test-benches of the 600 GHz doubler with two and four anodes are analyzed in this section. The epilayer thickness 200 nm doped at $2{\cdot}10^{17}$ cm^{-3} proposed in section 4.2.1 for the four anodes doubler chip is compared with the 350 nm epilayer thickness doped at $1{\cdot}10^{17}$ cm^{-3} for the two anodes chip version. The PSBD characteristics of the simulated devices are indicated in Table IV.3, where the considered built-in voltages fix the barrier height at 0.80 eV in both cases.

	Doping (cm^{-3})	W_{EP} (nm)	Area (μm^2)	η	I_{Sat} (pA)	R_S (Ω)	V_B (V)	C_{j0} (fF)	V_{BR} (V)
D0	$1{\cdot}10^{17}$	350	3.5	1.18	0.097	27	0.77	4.3	-7.5
D6	$2{\cdot}10^{17}$	200	3.24	1.2	0.194	11.2	0.79	5.46	-5.5

Table IV.3. Physical and geometrical properties of the PSBDs considered in the (D0) two anodes and (D6) the four anodes 600 GHz doubler chip designs presented in section 4.1 and 4.2 respectively.

We start comparing the conversion efficiency performed by each doubler at equivalent pumping conditions and then we thoroughly analyze the diode cell performances. The exact dimensions of the waveguide matching system of the block have been considered in our simulations, where the input and output curves used for the block alignment have been precisely simulated in HFSS (See Fig. 4.2).

4.2.3.1 Power Handle and Conversion Efficiency

We recall that the 600 GHz two anodes doubler chip was optimized for 10 mW of input LO power with 5 μm GaAs membrane while the four anodes chip has been optimized for 15 mW input power and a 4 μm membrane. The reduction of the membrane thickness has a negative impact on the amount of volume for heat dissipation but it has a positive impact on the reduction of the transmission losses in the chip. However, the best conversion efficiency of the two anodes doubler chip is performed when pumping each diode at ≈ 4.25 mW if 85 % LO coupling efficiency is considered, while this point is found at 3.2 mW per diode for the four anodes doubler chip. This indicates that the power distress in the four anodes version is lower than in the two anodes version, for each optimal input power, while it is still able to manage more input power. Additionally, the anode dimensions of the PSBDs used in each application are very similar, as indicated in Table IV, i.e., each PSBD in the four anodes version manage half of the power managed by each PSBD in the two diodes version. Additionally, equivalent maximum and minimum values of the current response have been obtained in both designs with ADS-HFSS simulations while the excited voltage signal is smaller in each PSBD of four anodes version, in accordance with the lower managed LO power. This should result in lower self-heating per diode and a more distributed temperature gradient in the four anodes chip. The global conversion efficiency and delivered output power of both chip versions are compared in Fig. 4.26. The global conversion efficiency is calculated by comparing the output power delivered with respect the input power. It contains

all losses associated with the input and output matching network of the device (see Fig. 5) as well as the conversion efficiency in the PSBDs. The output power is calculated in the exit of the mechanical block without considering any additional losses associated to any measurement device. Both versions of the 600 GHz doubler are compared when pumping with 10, 15 and 20 mW of input LO power which is the expected range, as show in section 3.2.4. The optimal bias for each chip version has been found for each considered input power. It is a -2, -2.6 and -3 V optimal bias for the four anodes chip and a -1.6, -2.2 and -2.8 V for the two anodes version when pumping at 10, 15 and 20 mW input power respectively.

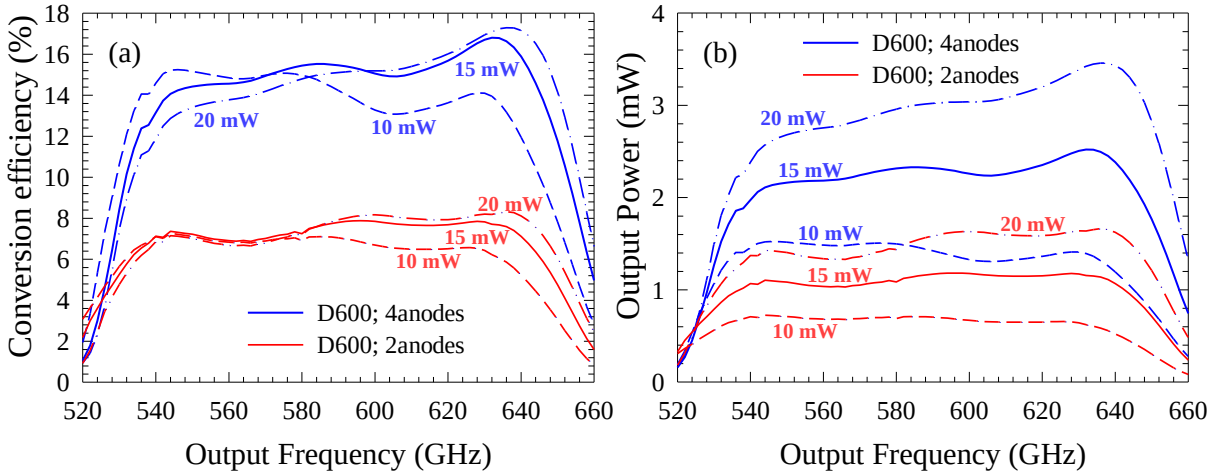

Fig. 4.26. Comparison of the simulated performances in ADS-HFSS simulations of the (a) global conversion efficiency and the (b) output power delivered by the 600 GHz doubler chips with four (blue lines) and two anodes (red lines). The results are obtained when pumping the devices with 10, 15 and 20 mW input power and biasing at -2, -2.6 and -3 V respectively for the four anodes chip and at -1.6, -2.2 and -2.8 V respectively for the two anodes chip.

Conversion efficiency between 13 – 16 % is predicted for the four anodes version while conversion efficiency between 6 – 8 % is found for the two anode version, in accordance with the experimental results presented in section 4.1. The delivered output power varies from 1.4 mW to 3 mW for the predicted performance of the new four anodes version when pumping from 10 mW to 20 mW of input power, compared with the 0.7 mW to 1.5 mW obtained by the two anodes version, as shown in Fig. 4.26.(b). It indicates that the global performance of the four anodes doubler has almost been increased by 100 %. It is also remarkable that the bias applied is very similar in both structures despite having twice the number of diodes in each version. It is because the required bias for each diode in the four anodes version is almost half of the bias required in the two anodes version due to the increased doping level. However, there are twice as many diodes in the four anodes version and the bias needs to be increased.

4.2.3.2 Impedance Matching Network

The coupling efficiency of the input signal and the output signal with the PSBDs of MMIC chip is one of the keys when optimizing sub-millimeter structures. However, the efficiency of the PSBDs to generate the second harmonic of the input signal is the most important point of the design. This is because the coupling efficiency of the input and output signals in these designs can be optimized between 75-85 % for the input power and 80-90 % for the output power in any set of diodes to be coupled in the diode cell of the chip. However, the higher the

second harmonic generation efficiency is in the coupled PSBDs, the higher the available power to be coupled with the output matching network. It is the reason for the analysis carried out in section 4.2.1 to determine a suitable PSBD structure for this application.

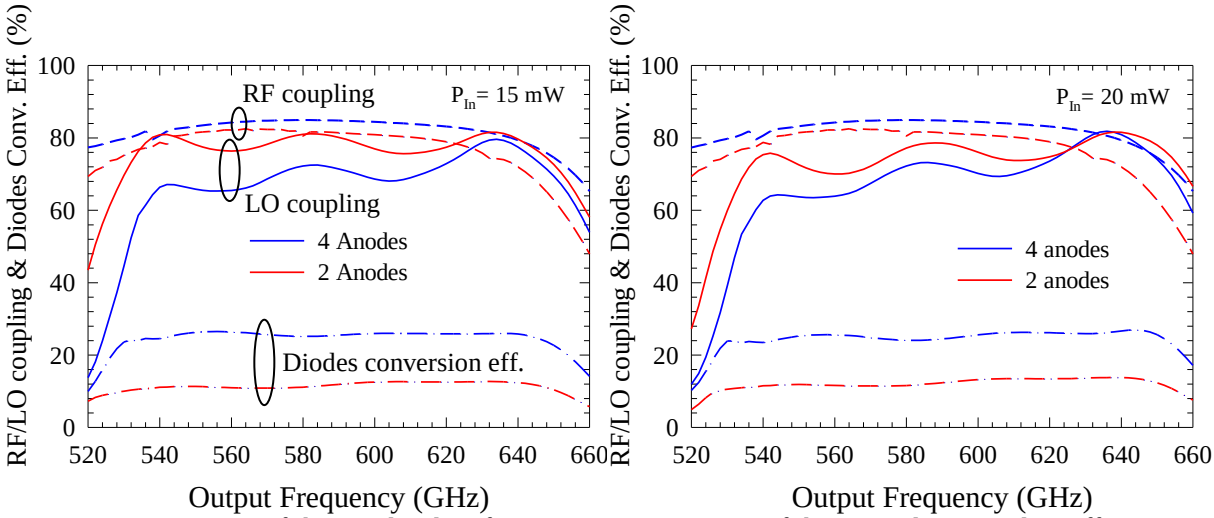

Fig. 4.27. Comparison of the simulated performances in ADS-HFSS of the LO and RF coupling efficiency and the second harmonic generation of the PSBDs in the 600 GHz doubler chips with four and two anodes. The results are obtained when pumping the devices with 15 and 20 mW input power and biasing at -2.6 and -3 V respectively for the four anodes chip and at -2.2 and -2.8 V respectively for the two anodes chip.

The LO and RF coupling of each chip version are compared in Fig. 4.27 when pumping with 15 mW and 20 mW of input power and biasing with -2.6 V and -3.0 V respectively for the four anodes version and -2.2 V and -2.8 V for the two anodes version. The considered bias is the optimal one that maximizes the global conversion efficiency of the device. We can conclude in Fig. 4.19 that the input signal coupling in the new four anodes version of the 600 GHz doubler is lower than the two anodes version design. It can be translated in -7 to -8 dB of return losses in the four anodes version compared with -9 to -11 dB of returns losses in the two anodes version, as plotted in Fig. 4.28. This is a non-desirable situation since the four anodes version is expected to couple up to 13 % less of input power in some points of the band with respect the two anodes version and it will also generate stronger standing waves in the four anodes version when connecting the 300 GHz power combine doubler, as presented in section 4.1.3. However, the second harmonic generation efficiency of the diode cell in the four anodes chip (22-25.5 %) is twice the efficiency of the diode cell in the two anodes version (11-12.2). This means that the second harmonic generation has been increased up to 100 % in most of the band. Additionally, the RF coupling efficiency is 4-5 % higher in the four anodes version in most of the band. This results in almost doubling the performance of the full 600 GHz four anodes doubler design (Fig. 4.26) with respect the two anodes one, in spite of having a lower available input power coupled with the PSBDs. This is because the four anodes version wastes up to 13 % more input power than the two anodes version, but it transforms the coupled input power two times better and the generated second harmonic is coupled 4-5 % more efficiently with the output stage of the device.

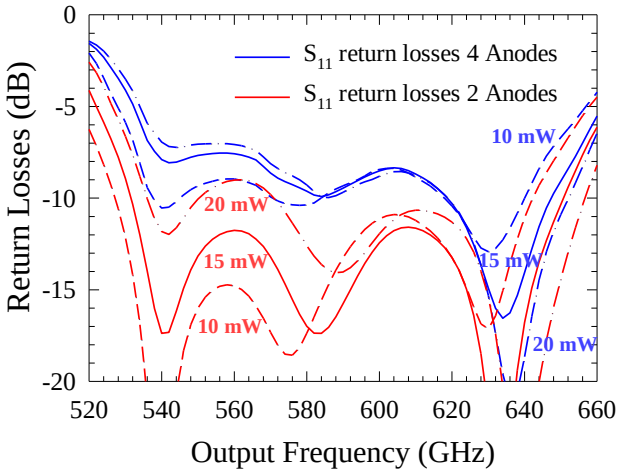

Fig. 4.28. Comparison of the simulated performances in ADS-HFSS of the return losses, calculated between the simulated input power and the reflected power in the input stage, of the 600 GHz doubler chips with four and two anodes. The results are obtained when pumping the devices with 10, 15 and 20 mW input power and biasing at -2, -2.6 and -3 V respectively for the four anodes chip and at -1.6, -2.2 and -2.8 V respectively for the two anodes chip.

4.2.4 Comparison with ADS-HFSS Individual Simulations

The experimental results obtained when measuring the output power, the DC component of the current in RF conditions, the estimated efficiency and the optimal bias of the 600 GHz two anodes doubler are compared here with ADS-HFSS simulations of the new 600 GHz four anodes doubler design. The 600 GHz four anodes doubler is simulated individually in this section using the developed SDD model. This means that no standing waves appear and the input power can be fixed. The considered input power is exhibited by the red line plotted in Fig. 4.6, i.e., the experimental output power delivered by the 300 GHz power combine doubler is considered in all simulations carried out in this section. The simulated input power is 0.3 dB higher than the measured values in Fig. 3.19 in order to correct the estimated transmission losses introduced by the calorimeter used in the measurements of the 300 GHz doubler. The simulated parameters are based on the modification of the anode size and the epilayer doping and thickness in accordance with the values obtained in Fig. 4.4. The saturation current $I_{Sat}= 2.06\cdot10^{-12}$ A, the ideality factor $\eta=1.3$, the built-in voltage $V_B= 0.75$ V T=295 K. The additional parameters of the model are $\alpha= 0.85$, $\beta= 0.64$, W_{EP}-$W_{CA}= 35$ nm and W_{CB}-$W_{EP}= 9$ nm. The new series resistance simulated in the SDD model is $R_S= 12\ \Omega$ and it is obtained from the experimental I-V characteristics in Fig. 4.4, when considering 200 nm of epilayer thickness and using the developed resistance model to approximate the experimental conversion efficiency of the device. It is important to mention that it has been concluded in the bibliography (Fig. 7 in [Graj00b]) that this frequency doubler, featuring $2\cdot10^{17}$cm^{-3} epilayer doping, input power from 270 GHz – 320 GHz and an average bias between -1 V and -2 V, is not affected by saturation phenomena of the carriers transport.

The results of the study can be found in Fig. 4.29, where the experimental values of the 600 GHz 2 anode doubler output power, the DC component of the current in RF conditions and the estimated efficiency are plotted in black lines. The ADS-HFSS simulation predictions have been obtained for each one of these magnitudes when fixing the 600 GHz 4 anodes doubler bias at -0.5 V (red lines), -1.0 V (blue lines), -1.5 V (green lines), -2 V (pink lines)

and -2.5 V (dark yellow lines). It is important to note that the 600 GHz 4 anodes doubler is individually simulated with the input power, given by the red line in Fig. 4.6, for all considered cases, thus no standing waves modifies the doubler performances. A 0.3 dB attenuator is used in the output of the simulated device in order to account for the estimated transmission losses in the PM5 calorimeter used in Fig. 4.5 for measuring the experimental 600 GHz 2 anodes doubler.

The optimal bias that optimizes the output power delivered by the 600 GHz four anodes doubler can be found in Fig. 4.16.(b), where it is possible to note that the maximal bias is around -1.4 V for each diode (~2.8 V for each branch). This is the reason for the considered values of the bias in the ADS-HFSS simulations from -0.5 V to -2.5 V. The predicted conversion efficiency of the new 600 GHz doubler design varies from 14 % in the middle of the band to 15-16 % in the edges of the band. We recall that the design presented in Fig. 4.18 was optimized for 15 mW of input power and therefore is over-pumped in accordance with the input power simulated for the study carried out in Fig. 4.29, which is exhibited in Fig. 4.6 by the red dashed line.

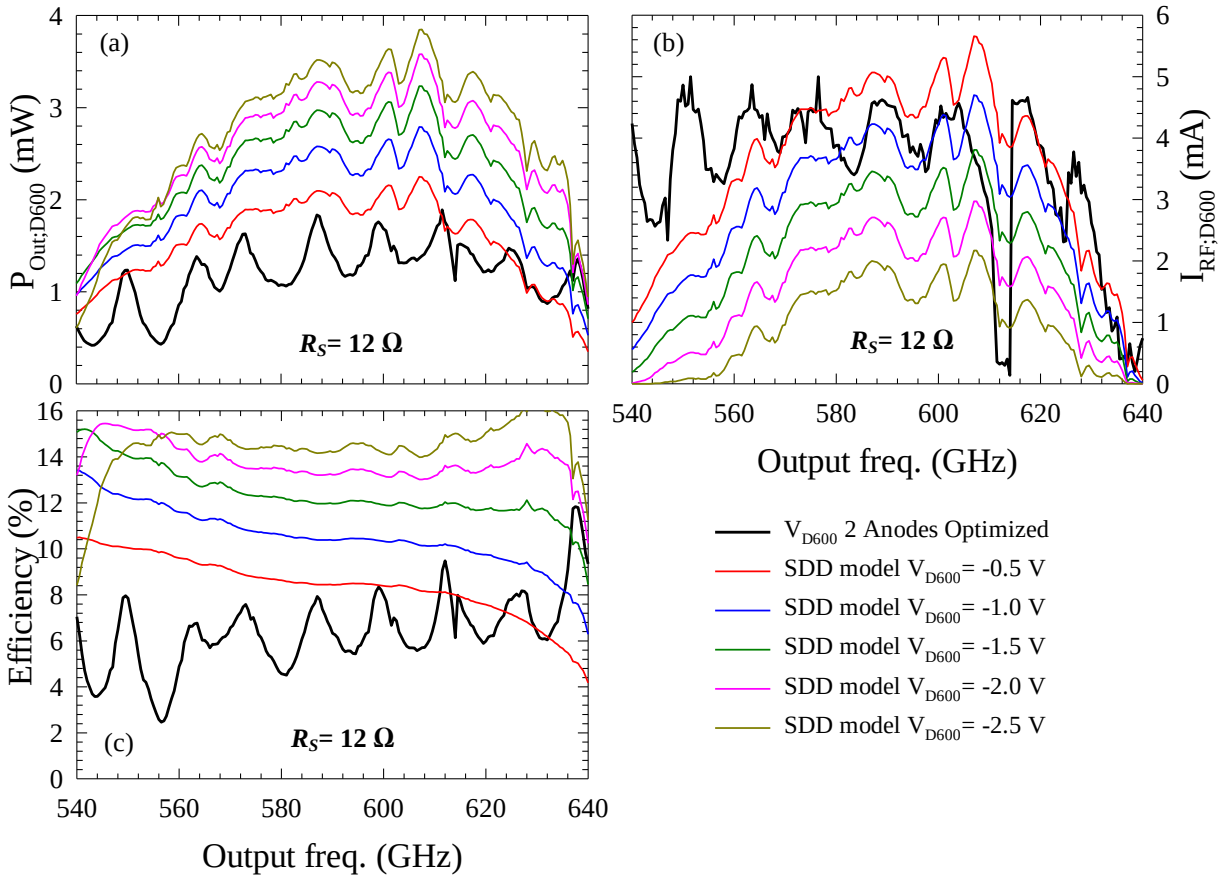

Fig. 4.29. Comparison between 600 GHz 4 anodes ADS-HFSS doubler simulations and the experimental 600 GHz 2 anodes doubler results (black lines) of (a) the output power, (b) the DC component of the current in RF conditions and (c) the conversion efficiency. The developed SDD model of the PSBDs has been used to predict the 600 GHz four anodes doubler performances when fixing the bias between -0.5 V (at low frequencies of the band) and -2.5 V (high frequencies of the band). Simulated R_S= 12 Ω. All figures are affected by the legend. Simulated T= 295 K.

However, the performance in the middle of the band can be increased up to 15 % using a reverse bias until -3.5 V where the breakdown voltage (~ -5.5 V) is predicted to be reached by the excited signal in accordance with the input power values at these frequencies. The depth of the epilayer in this design was optimized to manage a -4.5 V minimum excited voltage signal while the breakdown voltage is at lower values (~ -5.5 V). This means that a slight reduction in the conversion efficiency is predicted to be induced by the substrate effect model. However, this still enables an improvement in the final conversion efficiency.

Regarding the output power, it is expected to exceed 3 mW in the middle of the band and deliver at least 1.2 mW in the full frequency band. The presence of the standing waves will introduce oscillations in the delivered input power due to the variations of the effective input power, but at least 0.8 mW is expected in the minimum case. Finally, the DC component of the PSBDs in RF conditions is equivalent to the current performed by the 600 GHz 2 anodes version presented in Fig. 4.8.

4.2.5 Experimental Comparison with Combined Simulations of the 300 GHz and the 600 GHz four Anodes Doubler

The 300 GHz power combine doubler and the 600 GHz 4 anodes doubler are simultaneously simulated in this section in order to check the interaction between multiplication stages mediated by the standing waves. The standing waves are supposed to be stronger in this doubler due to the higher return losses presented in Fig. 4.28. The analysis carried out in section 4.1.5 is reproduced here for the new 600 GHz 4 anodes doubler design. The first analysis presented in Fig. 4.30 represents how the output power delivered by the 300 GHz power combine doubler is modified when connecting the 600 GHz four anodes doubler and how it affects the final output power delivered by the 600 GHz four anodes doubler. The output power delivered by the 600 GHz four anodes doubler is, once again, attenuated in 0.3 dB to take into account the estimated losses introduced by the PM5 calorimeter in the experimental measurements. The considered parameters of the PSBDs in the 300 GHz doubler are the same ones used by red dots in Fig. 3.20, i.e., saturation current I_{Sat}= 2.59·10^{-13} A, ideality factor η= 1.18, junction capacitance C_{j0}= 19.7 fF, built-in voltage V_B= 0.765 V, T= 295 K and series resistance R_S= 5.2 Ω. This means that the output power of the simulated 300 GHz doubler in the lower half of the band is smaller than the experimental one, but it does not modify the conclusions of this study. The considered parameters of the PSBDs in the 600 GHz four anodes doubler are the same ones used in section 4.2.5, i.e., I_{Sat}= 2.06·10^{-12} A, the ideality factor η=1.3, the built-in voltage V_B= 0.75 V and T=295 K. The secondary parameters used in both cases are α= 0.85, β= 0.64, W_{EP}-W_{CA}= 35 nm and W_{CB}-W_{EP}= 9 nm. The input power of the 300 GHz power combine is fixed in accordance with values experimentally found in Fig. 3.20.(a). The bias of the 300 GHz doubler is also fixed for each frequency reproducing the best performances of the output power given in Fig. 3.20.(a). The output power delivered by the 300 GHz doubler without connecting the 600 GHz four anodes doubler is exhibited by the black line in Fig. 4.30. The effective delivered power by the 300 GHz doubler (input power of the 600 GHz 4 anodes doubler), when connecting the 600 GHz 4 anodes doubler biased at -0.5 V (red line), -1.5 V (blue line) and -2.5 V (green line), is also plotted to study its modification.

It is important to note in Fig. 4.30.(a) that the effective input power of the 600 GHz four anodes doubler is significantly modified by its own polarization. The modification when biasing around -1.5 V is not as strong as it is when biasing with low reverse bias (-0.5 V) or high revers bias (-2.5 V) at these levels of input power. Although the effective input power is impacted by the interaction with the standing waves, it induces the highest effective input power at certain low frequencies when biasing at -0.5 V. It is also possible to remark that the maximums induced by the -0.5 V bias correspond with the minimums at -2.5 V. This basically indicates that the effective input power available in the 600 GHz four anodes doubler diodes depends on its bias. The final optimum bias of the 600 GHz four anodes doubler can be estimated in Fig. 4.30.(b) where the maximum output power results in a trade-off between the available input power and the efficiency of the diodes to generate the second harmonic at this optimum bias. A maximum output power of 3 mW is expected to be delivered by this new design of the 600 GHz doubler, which corresponds with a ~15 % maximum efficiency in accordance with the simulated effective input power. It is also expected that at least 1 mW of output power will be delivered even in the minimums induced by the standing waves. It is important to recall that the nominal simulated input power of the 600 GHz doubler, black line in Fig. 4.30.(a), is smaller than the experimental one in the lower half of the band (see Fig. 3.20).

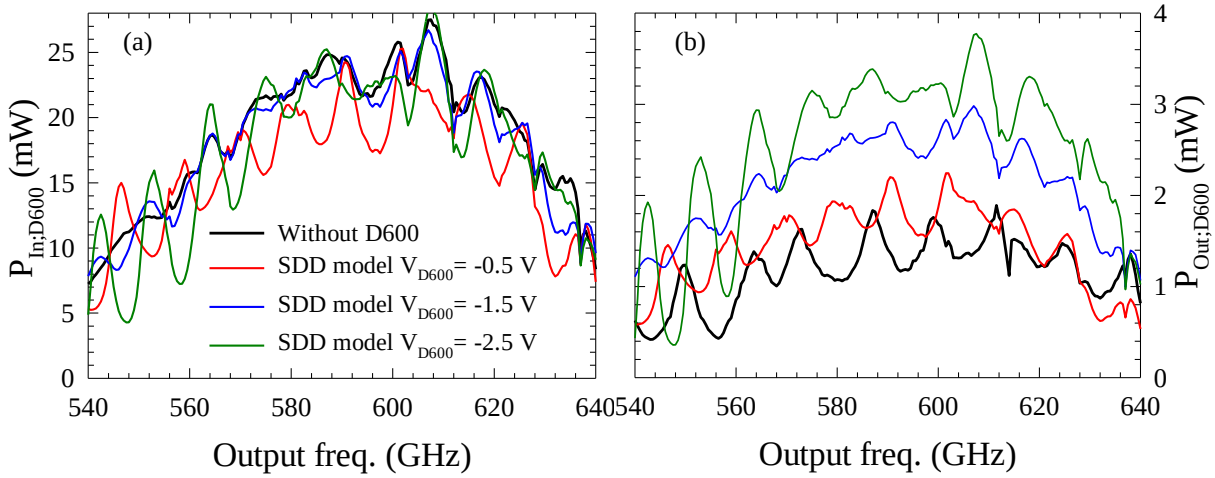

Fig. 4.30. Comparison between the simulated output power by (a) the 300 GHz power combine doubler without (black line) connecting the 600 GHz 4 anodes doubler and (b) the delivered power by the simulated 600 GHz 4 anodes doubler when it is connected and biased at -0.5 V (red line), -1.5 V (blue line) and -2.5 V (green line). The input power of the 300 GHz doubler is fixed with the values given in Fig. 3.19. The legend affects both Figures. The experimental output power obtained with the 600 GHz 2 anodes doubler (black line) is given in figure (b) as a reference.

A remarkable discrepancy can be observed between these simulation results and the experimental results presented in Fig. 4.7. The experimental oscillations are correctly predicted by ADS-HFSS simulations. However, simulations also predict a displacement of the maximums of the output power when sweeping the bias, but it does not correspond to the experimental behavior observed in Fig. 4.7. It was previously advanced that the standing waves between the 600 GHz doubler and the 300 GHz doubler affect also the effective input power delivered into the 300 GHz by the RPG source. It is possible to extract this conclusion when analyzing the conversion efficiencies of each doubler in accordance with the simulation results obtained in Fig. 4.30. The conversion efficiencies of each doubler are plotted in Fig

4.31 where the conversion efficiency of the 600 GHz four anodes doubler is directly calculated between its delivered output power (without the 0.3 dB attenuation) and the effective input power. The conversion efficiency of the 300 GHz doubler is obtained between the effective delivered power and the simulated fixed input power. The first interesting point to highlight in Fig. 4.31 is the flat conversion efficiency performed by the 600 GHz four anodes doubler. This takes place despite the strong variations in the effective input power, while the conversion efficiency of the 300 GHz doubler features the standing waves oscillations. This means that the modifications induced by the standing waves in the effective input power of the 600 GHz four anodes doubler are strongly related to the capacity of the 600 GHz four anodes doubler diodes to couple with the incoming LO power. Both doublers were individually optimized to feature a flat coupling capacity along the band, but the presence of standing waves induces the oscillation of the matching impedance of the diode cell around the optimized one. This results in an interaction with the standing waves along the band which induces an effective input power in the 600 GHz doubler that keeps the conversion efficiency of the doubler unmodified along the band. However, a fixed input power is imposed on the 300 GHz doubler, thus the oscillations of the conversion efficiency featured by the 300 GHz doubler are associated to the way the standing waves modify the capacity of the PSBDs to match the generated second harmonic with the RF antenna. The new 600 GHz 4 anodes doubler is expected to perform 12-15 % conversion efficiency along the frequency band in spite of the influence of standing waves between the multiplication stages.

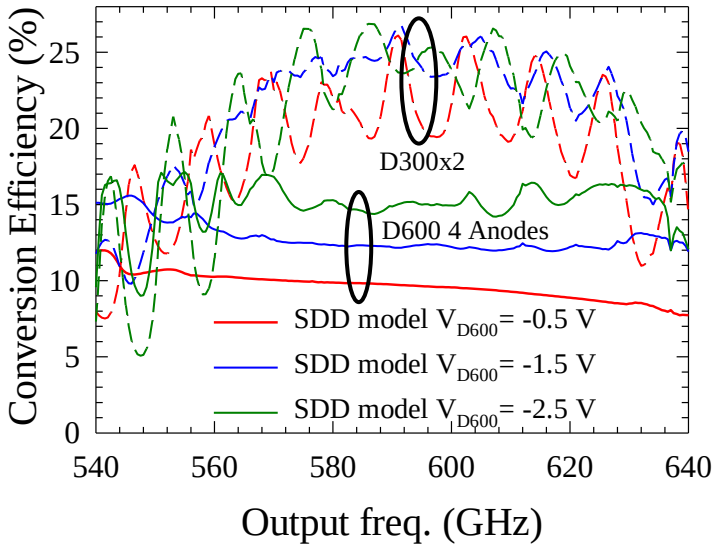

Fig. 4.31. Conversion efficiency obtained in ADS-HFSS simulations of the (a) 300 GHz power combine doubler and the (b) 600 GHz doubler when they are simultaneously simulated. A fixed set of input power and bias values are defined for the 300 GHz doubler in accordance with Fig. 3.19.

Given these results, we conclude that the effective input power delivered by the RPG source to the 300 GHz doubler is also modified in a way that softens the effective conversion efficiency of the 300 GHz doubler plotted in Fig. 4.31.(a). This explains the experimental constant position of the maximums and minimums in Fig. 4.7, since the coupling capabilities of PSBDs in the 600 GHz and 300 GHz doublers are modified at the same time by standing waves. This study has demonstrated that a lower reverse bias (-0.5 V) of the 600 GHz four anodes doubler is able to deliver a higher output power when simulating both multiplication

stages simultaneously, due to the presence of standing waves between doublers. This behavior is able to modify the tendency obtained by single simulations in Fig. 4.8, where higher reverse biases (~ 2 V) were always predicted to be better. It is due to a trade-off between the conversion efficiency of the 600 GHz 4 anodes doubler at each bias and the available effective input power when sweeping its bias.

4.3 Conclusions

A 600 GHz two-anodes doubler designed by Dr. F. Yang and presented in section 4.1 has been developed using the LERMA-LPN process, resulting in a functional device able to deliver up to ~1.5 mW using the LO source presented in Chapter 3. The experimental results have been analyzed in section 4.1.4 in terms of the ADS-HFSS simulations using the developed SDD model, which has shown maximum conversion efficiency around 7-8 % along the frequency band. Also, a significant influence of standing waves between the multiplications stages have been found and analyzed in section 4.1.5. The experimental maximum output power is around 1.9 mW in the middle of the band but it drops under 0.5 mW at certain low frequencies. This is due to the lack of input power delivered by the 300 GHz power combine doubler together with the influence of the standing waves on the effective input power delivered into the 600 GHz two-anodes doubler.

A new design of a 600 GHz four-anodes doubler proposed by this author has been detailed in section 4.2, starting with an analysis of the PSBDs properties for this specific application in section 4.2.1. The comparison between the 600 GHz two-anodes and 600 GHz four-anodes doublers has been carried out in section 4.2.3. Analysis of the realistic performances that can be experimentally achieved by the new 600 GHz four-anodes doubler has been carried out in sections 4.2.5 and 4.2.6, based on experimental measurements of the 300 GHz LO chain. The estimated conversion efficiency performed by the new design is around 12-15 % in the full band and at least 1 mW of output power between 540 GHz and 640 GHz is expected in spite of the standing waves presence. A maximum value of output power around 3 mW is expected to be delivered by the experimental device.

5 A 600 GHz Frequency Receiver

A 600 GHz sub-harmonic unbiased frequency mixer was developed by Dr. J. Treuttel at LERMA using a 3D-electromagnetic simulator (Ansys, HFSS) and a non-linear harmonic balance simulator (Agilent, ADS) following the procedure presented in section 1.2. It was fabricated using the LERMA-LPN Schottky process [Treut14] and the results at room and cryogenic temperatures have been published in [Treut16] and [Maes15]. This mixer was developed within the framework of the JUICE-SWI mission in order to fulfill the 600 GHz channel specifications. The mixer covers the frequency range from 520-620 GHz and is pumped by the 300 GHz doubler presented in chapter 3, forming the ensemble of the 600 GHz receiver proposal indicated in Fig. 1.2. A 1500 K double side band (DSB) noise temperature of the receiver at 120 K cryogenic temperature was specified by the project requirements. However, an average of 1284 K DSB noise temperature has been performed by LERMA's receiver at room temperature, and a minimum value of 1130 K DSB was achieved at 557 GHz. An average of 685 K DSB receiver noise temperature was achieved at 134 K ambient temperature and a minimum value of 585 K was achieved at 540 GHz. The noise temperature specifications of the project have been improved by this 600 GHz receiver by a factor two.

The objective of this chapter is to analyze the main characteristics of the 600 GHz frequency receiver design in terms of the developed physical model of the PSBDs in order to determine the origin of such positive results. The device is already thoroughly described and presented in [Treut16] and [Maes15], and we therefore focus the analysis on the properties of the PSBDs used in this application and the relationship with the matching network of the MMIC chip. We start presenting the conditions of the PSBDs in the full ADS-HFSS simulations of the 600 GHz mixer and then, the ideal diodes performances are analyzed and related with global simulations in terms of the developed PSBDs physical model. The conclusions extracted from this analysis are then implemented in the decision making of the 1.2 THz mixer.

5.1 Qualitative Description of the Device

The virtual design in HFSS is presented in Fig. 5.1. The full description of this device is explained in [Treut16] and [Maes15], and brief descriptions of the main points for the purpose of this section are discussed here. In this chapter we analyze the relationship between the performances of the PSBDs in the antiparallel configuration and the impedance matching network, which consist of the transmission lines, filters, antennas and the waveguides system. The main structures of the 600 GHz MMIC mixer chip are indicated in Fig. 5.1, where the antiparallel configuration of the PSBDs in the diode cell is a key aspect of the analysis carried out in this chapter. The diode cell is coupled in this case with the quasi-TEM mode of both the LO and the RF signals. This means that the PSBDs present exactly the same antiparallel configuration for both signals, in contrast with the different configuration presented by the diodes for each signal in the doubler designs presented in chapters 4 and 5. The excited signal in the PSBDs by both the LO and RF signals is exactly the same but it presents a 180 degree shift between each diode of the cell. However, the diodes are also in antiparallel configuration

for any generated harmonic or intermodulation product [Manl56], [Rowe58], [Pant58], [Pepp68] of the LO and the RF signal. This means that the odd harmonics and intermodulation products are now generated in phase by each PSBD of the diode cell while the even harmonics and intermodulation products are generated in opposite phase due to the antiparallel configuration of the PSBDs. The even harmonics and intermodulation products cancel each other out in the diode cell while the odd harmonics and intermodulation products come out of the diode cell. This anti-parallel configuration can be found in the bibliography in [Mehd98], [Cheng12], [Sobi14] and it is discussed together with the 600 GHz sub-harmonic mixer in this chapter, since the intermediate (IF) signal is an odd intermodulation product of frequency $2 \cdot f_{LO} - f_{RF}$ and $-2 \cdot f_{LO} + f_{RF}$. A variation of this anti-parallel configuration can also be found for sub-harmonic mixers design in [Thom12], [Schl14], but it is especially widespread in frequency tripler devices [Maes05a], [Maes06], [Maes08], [Maes10a], [Maes10b], [Maes12] and [Sile15]. However, the signal treatment is much more complex in frequency mixing applications, since the excited signal in the diode cell by both the LO and RF signals, as well as all odd harmonics and intermodulation products, interact with the matching network system surrounding the diode cell. All of these generated signals define the final IF generation efficiency. The main signals to be treated in the design of this mixer are the LO signal, the RF signal, the IF signal and the third harmonic of the LO signal, which will be discussed in chapter 5 for the 1.2 THz mixer development.

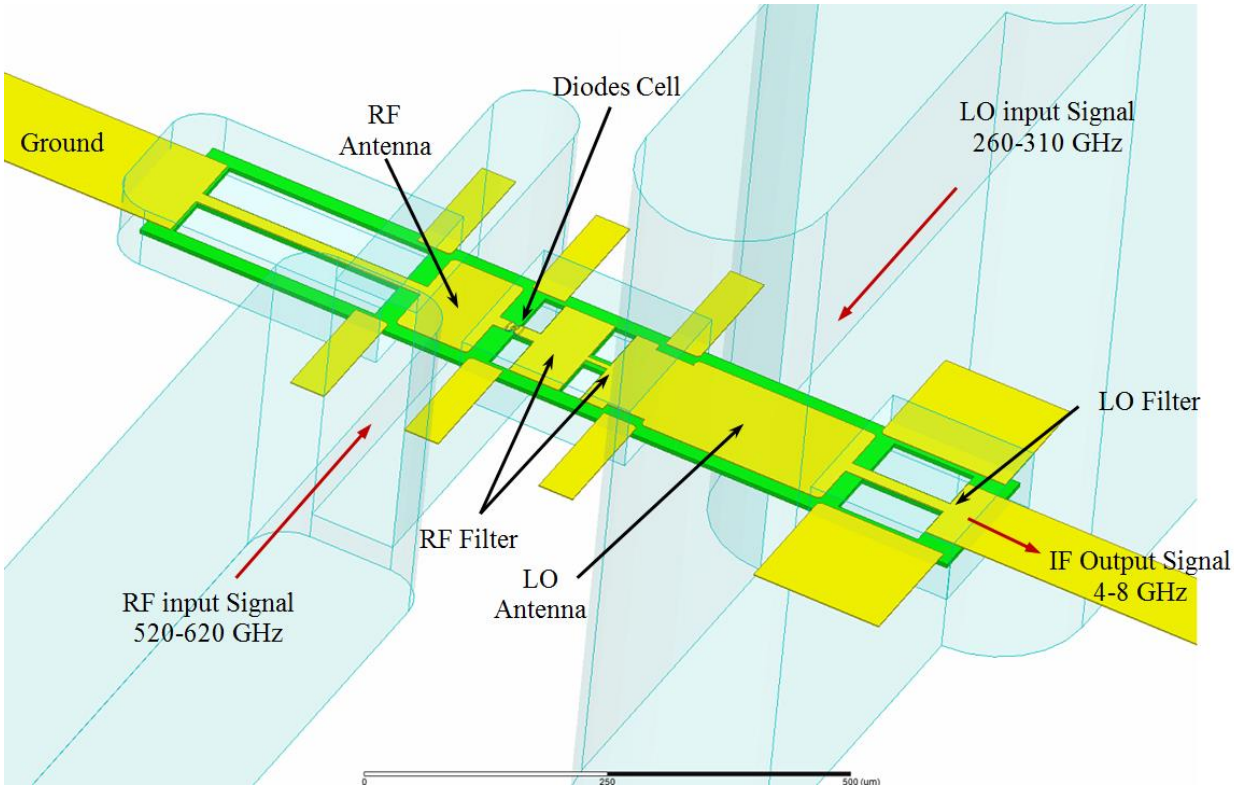

Fig. 5.1. Virtual design in HFSS of the front-end 600 GHz sub-harmonic frequency mixer. The diodes present an antiparallel configuration.

The LO signal arrives into the chip by coupling the TE_{01} mode propagated in the LO input waveguide with the LO antenna. The reflected LO signal by the LO filter and the coupled LO signal with the antenna have to be correctly in phase to propagate toward the diode cell. The LO signal crosses the RF filter and is reflected by the ground structure. The distance between

the diode cell, the ground and the LO filter has to be adequate to have a standing wave of frequency f_{LO} place in the proximities of the diode cell with an adequate impedance to couple the LO signal. The RF signal is coupled with the RF antenna and reflected by the low pass RF filter and the ground. The reflected RF signals by the ground structure and the RF filter have to generate a standing wave of frequency f_{RF} in the proximities of the diode cell with an adequate impedance to couple the RF signal. The generated odd harmonics and intermodulation products emerge from the diode cell and are propagated in the MMIC chip. The desired IF signal is extracted from the opposite side of the grounded side by designing a specialized IF adapter circuit. An IF adapter circuit has been designed from 250 Ω to 50 Ω for this application. The PSBDs perform a 55 nm epilayer thickness doped at $3 \cdot 10^{17}$ cm^{-3}. The anode size is $A \approx 0.5$ μm^2 which gives a junction capacity $C_{j0} \approx 1.2$ fF, a saturation current $I_{Sat} \approx 4.2 \cdot 10^{-12}$ A, an ideality factor $\eta \approx 1.34$ and a DC series resistance $R_S \approx 35$ Ω.

The interaction between the signals in these kinds of devices is extremely complex since the matching network of the diode cell is common to both the LO and RF signals. It means that it is not possible, and it is not required, to perfectly match the diode cell with both the LO and the RF signals. The final performance of the MMIC chip is the result of a trade-off between the LO and RF signals interaction to obtain the best IF generation of the device. A good IF adapter circuit would be also required to reduce as much as possible the losses of the generated IF signal between the diode cell and the output connector at 50 Ω.

5.1.1 IF Adapter Circuit

The IF adapter circuit results also in the trade-off between the maximal IF generation enhanced by the IF impedance Z_{IF}, imposed to the diode cell, and the efficiency of the IF circuit to adapt the Z_{IF} impedance with the nominal 50 Ω of the output connector in the required frequency band (from 4 to 8 GHz).

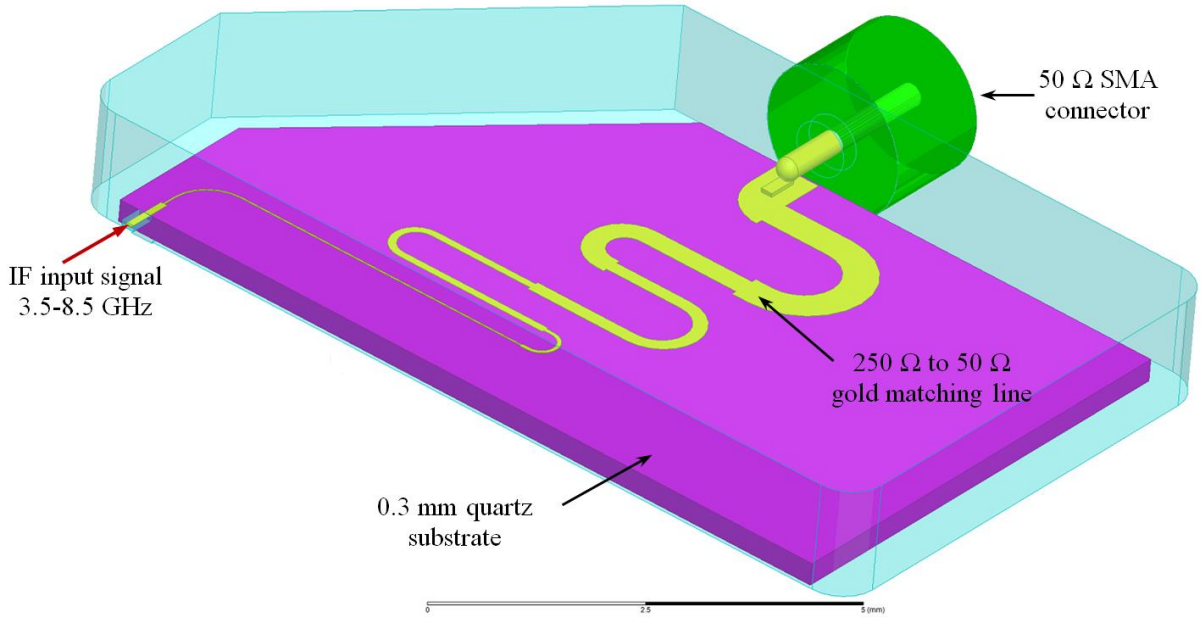

Fig. 5.2. HFSS design of the 3.5-8.5 GHz IF adapter circuit used in the front-end 600 GHz subharmonic frequency mixer. It has been optimized to adapt a 250 Ω IF impedance with the 50 Ω impedance of the SMA connector.

It has been concluded during this work that the higher the IF impedance, the higher the IF generation in the diode cell, but the lower the transmission of the generated IF signal in the IF adapter circuit. The HFSS design of the IF adapter circuit used in the front-end 600 GHz sub-harmonic mixer is presented in Fig. 5.2. It consists of a 1.7-µm-thick gold line on a 300-µm-thick quartz substrate that adapts the 250 Ω impedance of the input IF signal to the nominal 50 Ω impedance of the SMA connector. The S-parameters obtained in the HFSS simulation when connecting a 250 Ω load in port 1 (IF input signal) and a 50 Ω load in port 2 (connector) are plotted in Fig. 5.3. The transmission losses S(1,2) in the IF adapter circuit are between 0.3 to 0.5 dB while the return losses S(1,1) are lower than 15 dB in the full IF band and lower than 30 dB in some regions of the band. The performance of this IF adapter circuit will be used in the IF circuit design of the 1.2 THz subharmonic mixer presented in chapter 5.

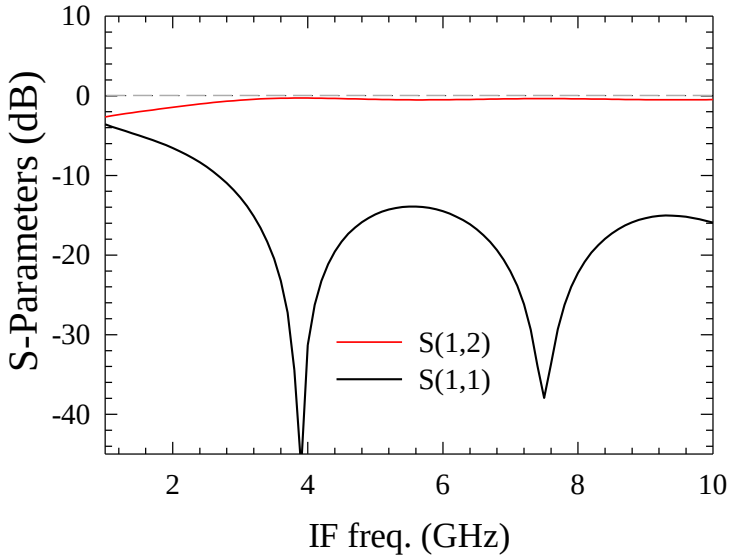

Fig. 5.3. HFSS results of the S-parameters given by the defined IF adapter circuit in Fig. 5.2. A 250 Ω impedance has been defined in port 1 (IF input signal) and 50 Ω in port 2 (connector). The IF transmission in the adapter circuit is between -0.3 to -0.5 dB.

5.2 Analysis of the PSBDs Impedance Matching in the 600 GHz Mixer

We present in this section the virtual ADS-HFSS performances of the LERMA-LPN subharmonic Mixer presented in [Treut16]. The analysis is focused on the signal's interaction with the PSBDs where the developed SDD model has been included accounting for the fringing and substrate effects. The physical and geometrical parameters defined in the SDD model are a 0.5 µm^2 anode surface, a 55-µm-thick epilayer doped at $3\cdot10^{17}$cm^{-3}, a built-in voltage V_B= 0.718 V, a saturation current I_{Sat}= $2.2\cdot10^{-12}$ A, an ideality factor η=1.34, an α=0.72 and a series resistance R_S= 35 Ω. Regarding the substrate effect parameters, the width of the substrate-epilayer junction has been defined by W_{EP}-W_{CA}= 28 nm and W_{CB}-W_{EP}= 9 nm.

The global HFSS simulations of the mixer structure presented in Fig. 5.1 have been used at LO, 3·LO, RF and IF frequencies. A fixed IF frequency at f_{IF}= 4 GHz is fixed for the analysis. The LO signal arrives to the simulated structure at LO frequencies (250-350 GHz) and any LO power arriving to the IF circuit is considered to be lost. The RF signal arrives to the

simulated structure at RF frequencies (500-700 GHz) where a $f_{RF}=2\cdot f_{LO}-f_{IF}$ is simulated and any RF power arriving to the IF circuit is considered to be lost. The signals are mixed in the diode cell and the resulting IF signal and intermodulation products heads to the simulated IF adapter circuit. The only additional frequency which has been included in these simulations is the third harmonic. It was not considered during the design of the MMIC mixer chip because it doesn't have a dramatic impact on the optimization of the device but it can have an impact in the IF generation efficiency in the diode cell due to the standing waves of the third harmonic in the MMIC chip. The third harmonic has been simulated in the structure (750-1000 GHz) and any third harmonic power arriving to the IF circuit is considered to be lost. The simulation of the third harmonic in the HFSS design of the MMIC chip has been found to be critical in the double side band (DSB) noise temperature predictions of the mixer, but it can be neglected in the optimization of the mixer chip. If the third harmonic is not simulated in HFSS, it is generated in the diode cell depending on the impedance used in the ADS test bench to extract it, and upper harmonics, from the simulation. It affects to the IF conversion efficiency, thus the final DSB noise temperature. Nevertheless, the third harmonic can be neglected during the optimization of the chip geometry since the influence of the non-simulated HFSS third harmonic on the IF generation has been observed to be equivalent in the full band for a given resistance use to extract it from the simulations. Once the chip is finished, a final third harmonic simulation is required in order to correctly simulate the noise temperature in the diode cell.

We now analyze the coupled LO power in the diode cell of the 600 GHz MMIC mixer that performs the best conversion efficiency of the RF signal into the IF signal. The coupled LO power and the conversion efficiency of the RF into the IF signal in the diode cell are plotted in Fig. 5.4 when varying the global input LO power from 1.8 mW to 2.8 mW. The global input RF power has been fixed at 10 µW in all cases, but it does not have a notably impact in the global performance of the mixer as long as it is much smaller than the coupled LO power in the PSBDs.

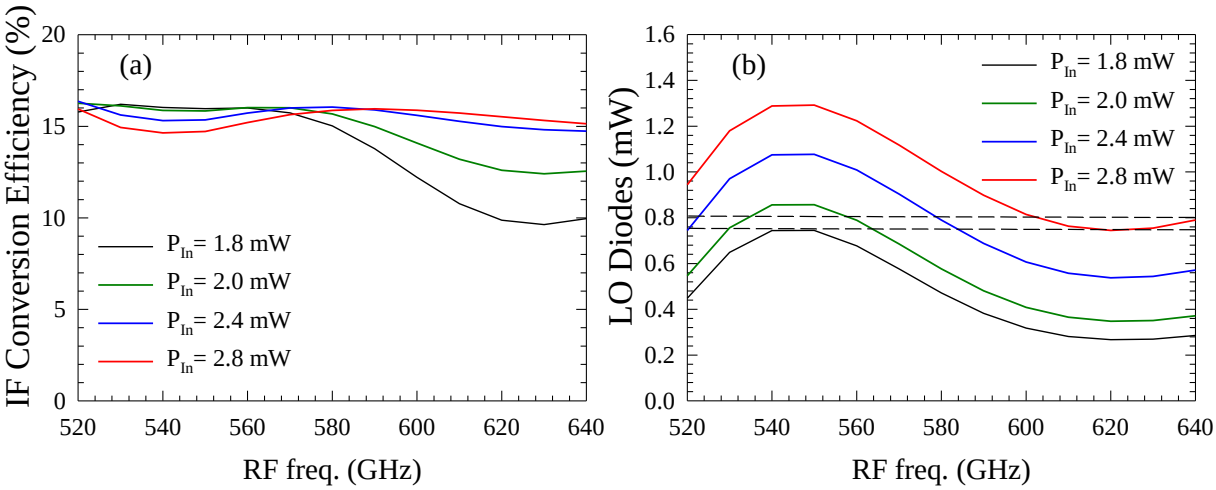

Fig. 5.4. HFSS results of the diode cell (a) conversion efficiency of the RF into the 4 GHz IF signal and (b) the LO power coupled with the diode cell when sweeping the input LO power from 1.8mW to 2.8 mW.

The best conversion efficiency along the frequency band can be observed in Fig. 5.4.(a) and it goes from 1.8 mW of input LO power at low frequencies of the band to 2.8 mW at high

frequencies of the band. However, it is translated into a coupled LO power in the PSBDs which has been modulated in the full band by the LO matching network of the MMIC chip to obtain an optimal coupled LO power around 0.76 mW in the diode cell, as observed in Fig. 5.4.(b). It is the minimum LO power, as we conclude in next section, that this structure has been able to couple with the PSBDs while optimally generating a 250 Ω IF signal from the coupled RF signal. The third harmonic has been included in the final analysis of the mixer performance since the average third harmonic power along the band is ~10^{-6} W while the generated IF power is ~10^{-7} W when simulating 10 µW of RF power, but it doesn't have an appreciable influence on the mixer performance. All other harmonics and recombination products powers are at least ten times lower than the generated IF power. The final IF power available depends on the coupled RF power in the diode cell and the transmission losses introduced by the IF adapter circuit. The percentage of RF power coupled in the diode cell is plotted in Fig. 5.5. We can see that the available RF power in the diodes to be mixed with the LO power does not vary as much as the LO coupled power when fluctuating the input LO power. The optimal RF coupling varies from 68 % to 78 % of the simulated RF input power (10 µW) along the band. The generated IF signal in the diodes has to finally go through the IF adapter circuit which introduces 0.3-0.5 dB of transmission losses, as indicated in Fig. 5.3.

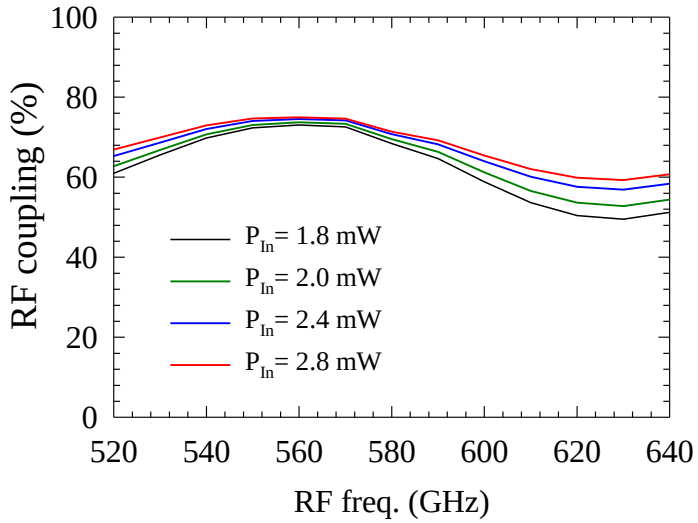

Fig. 5.5. HFSS results of the RF coupling in the diode cell when sweeping the input LO power from 1.8mW to 2.8 mW. A IF frequency fixed at 4 GHz is simulated.

The results obtained in this section allow us to understand the complex interaction of the LO and RF signals to generate the IF signal. The results obtained in Figs. 5.4 and 5.5 indicate that there is a minimum LO coupled power (~0.76 mW), as we conclude in next section, which matches as well as possible the RF signal captured by the RF antenna to optimally generate a 250 Ω IF signal at 4 GHz. Finally, it is necessary to study the ideal performance of these PSBDs in the considered frequency range.

5.3 Analysis of the PSBDs Performances

We discuss in this section the performances than can ideally be obtained by the PSBDs used in the device presented in [Treut16] and some variations of the anode size in the proximities of the nominal one. This analysis is similar to the analysis carried out in section 4.2.1. However it cannot be performed by considering a single PSBD because the IF signal generation depends not only on the coupled LO signal but also on the coupled RF signal. Two PSBDs in antiparallel configuration are therefore simulated in an ADS test-bench in this case to reproduce a simplified system which represents the diode cell used in the design presented in Fig. 5.1. We focus the analysis of this antiparallel configuration on two main points. First, we optimize the LO impedance of the simulated LO source for a specific frequency to fix the coupled LO power in the diode cell. Then we optimize the simulated RF source impedance to maximized the IF generation coupled with a 250 Ω IF impedance. We fix the IF frequency at 4 GHz which is the difference between the second harmonic of the LO signal and the RF signal. A 250 Ω impedance is fixed in the IF output port to extract the IF signal which strongly affects the interaction between the LO and the RF signals to deliver the correct IF signal. Second, we analyze the stability of the IF generation when introducing a RF mismatch in the diode cell. The first analysis enables us to identify the optimal LO power that can potentially deliver the maximal performance of the PSBDs. However, the second analysis enables us to identify the feasibility of a MMIC structure able to couple the LO and the RF signal in that optimal point. The analysis has been carried out for PSBDs with a doped epilayer at $3{\cdot}10^{17}$ cm^{-3}, varying the anode size to compare the performances with the nominal design used in the presented 600 GHz subharmonic mixer. A second analysis is presented when utilizing an epilayer doped at $5{\cdot}10^{17}$ cm^{-3} to determine the new PSBDs properties required to improve the performances of the 600 GHz mixer.

5.3.1 Analysis of the $3{\cdot}10^{17}$ cm^{-3} Epilayer Doping

The nominal structure considered in this analysis is the same one described in section 5.2 but it is also compared with two variations of the anode size, as indicated in Table V.1, to compare the tendency of the performance in other hypothetical applications. The parameters indicated in Table V.1 have been used in the developed SDD model accounting for the fringing and substrate effects explained in chapter 2, where a factor β= 0.64 is used in all simulations accounting for the surface charge influence on the PSBDs capacitance model.

	Doping (cm^{-3})	W_{EP} (nm)	Area (μm^2)	I_{Sat} (pA)	η	R_S (Ω)	V_B (V)	C_{j0} (fF)
D0	$3{\cdot}10^{17}$	55	0.60	2.62	1.34	29.2	0.718	1.43
D1	$3{\cdot}10^{17}$	55	0.50	2.20	1.34	35.0	0.718	1.22
D2	$3{\cdot}10^{17}$	55	0.42	1.84	1.34	41.6	0.718	1.03

Table V.1. Physical and geometrical properties of the PSBDs considered in the analysis for a 600 GHz subharmonic mixer. The defined diode D1 is the same diode used in 600 GHz mixer presented in section 5.1 but the diodes D0 and D2 present a different anode size. A built-in voltage V_B= 0.718 V, η=1.34, α=0.6, W_{EP}-W_{CA}= 28 nm, W_{EP}+W_{CB}= 9 nm and β= 0.64 are considered in all cases.

We start analyzing the maximal conversion efficiency of the RF signal into IF signal by the diode cell, using the nominal PSBD structure D1 described in Table V.1. The maximum

conversion efficiency of the diode cell when ideally coupling the LO power and optimizing the RF impedance that maximizes the IF generation (Z_{IF}= 250 Ω), for each coupled LO power, are plotted in Fig. 5.6 for the LO frequencies 260 GHz, 295 GHz and 320 GHz. We can see that the optimal coupled LO power in the diode cell is between 0.3 – 0.4 mW and the maximal conversion efficiency is reduced as the LO frequency is increased. Similar conversion efficiencies are obtained in the full band if higher values of coupled LO power are considered. These results can explain the observed tendency of the conversion efficiency plotted in Fig. 5.4.(b). Regarding the real part of the LO and RF ideal impedances presented in Fig. 5.6.(b), similar values are observed in both the LO and the RF signals at 0.4 mW of coupled LO power. It can be very hard to find a real MMIC chip able to couple the diode cell with a very similar real part of the LO and RF impedances, since the LO and RF matching network is the same in the proximities of the diode cell. However, the difference between the real part of both signals increases as the coupled LO power rises, heightening the feasibility of a MMIC circuit able to match both signals in the optimal point. Additionally, the ideal real part of the RF signal is stabilized as the coupled LO power rises.

We can conclude with this analysis that the final LO power coupled with the diode cell in the 600 GHz mixer presented in Fig. 5.1, is the smallest coupled LO power that allows the MMIC chip to adequately match the RF signal and maximize the generation of a 250 Ω IF signal at 4 GHz. This explains the ~0.78 mW of coupled LO power found in section 5.2.

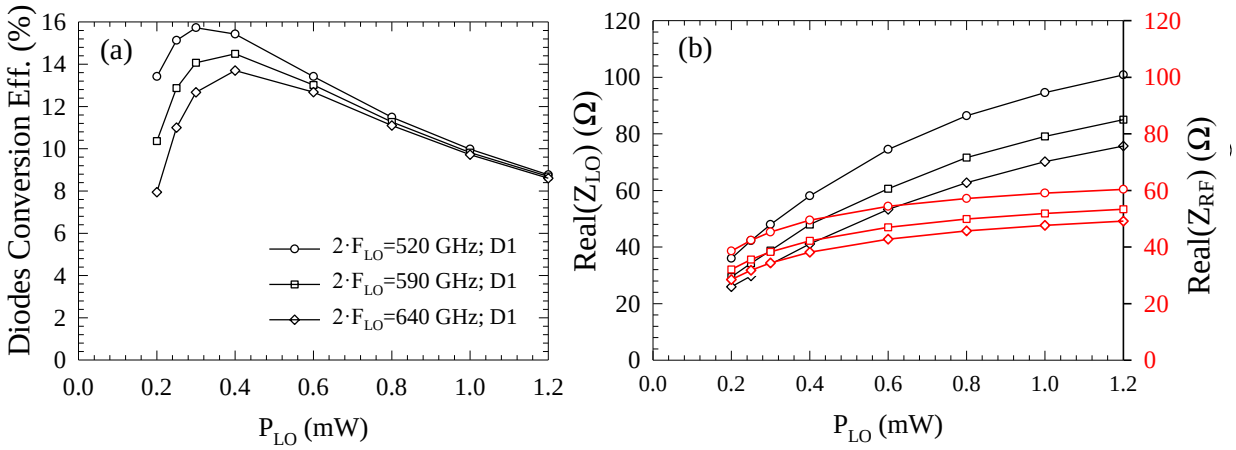

Fig. 5.6. ADS simulations of two PSBDs in antiparallel configuration with the D1 parameters indicated in Table V.1. It is the (a) ideal conversion efficiency of the RF into the IF signal and (b) the optimized real LO and RF impedances when sweeping the coupled LO power at LO frequencies 260 GHz, 295 GHz and 320 GHz. The legend affects to both figures.

We extend this analysis to the additional PSBD structures defined in Table V.1. The aim of this study is to compare the performances that could be obtained using another anode size. We can repeat the same analysis carried out in Fig. 5.6 for each diode proposed in Table V.1 for a fixed LO frequency at 320 GHz. The maximum conversion efficiency of the RF signal into the IF signal and the required real parts of the LO and the RF signals when sweeping the coupled LO power are plotted in Fig. 5.6 for the three PSBDs indicated in Table V.1. We recall that D0 presents the biggest anode size (0.6 μm^2), D1 is the nominal structure with (0.5 μm^2) and D2 the smallest one (0.42 μm^2).

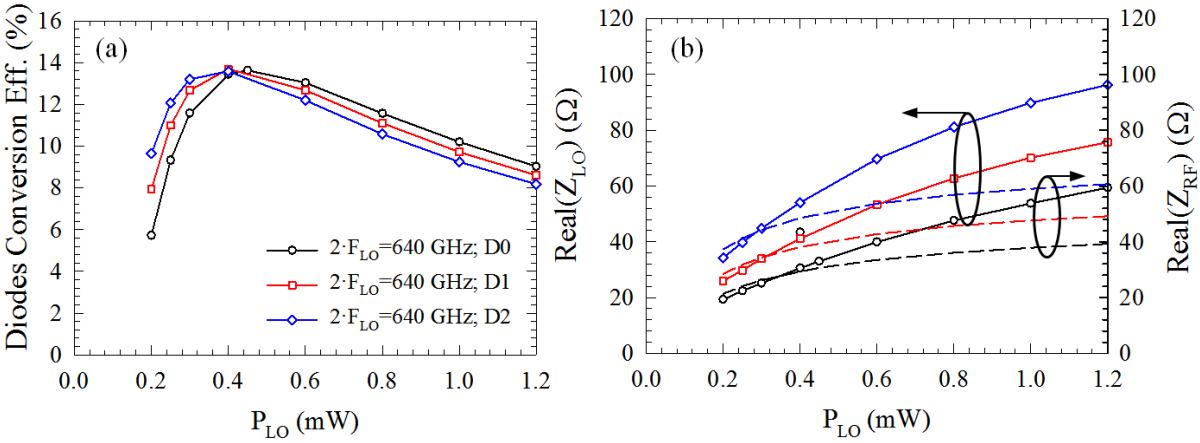

Fig. 5.7. ADS simulations of two PSBDs in antiparallel configuration for the three diodes indicated in Table V.1. It is the (a) ideal conversion efficiency of the RF into the IF signal and (b) the optimized real LO and RF impedances when sweeping the coupled LO power at 320 GHz LO frequency. The legend affects to both figures.

It is important to note that the equivalent maximum conversion efficiency in all considered diodes is around 0.4 mW of coupled LO power when fixing the epilayer doping. The ideal coupled LO power for each anode decreases as the anode size decreases due to the reduction of the charge under the anode. However, the maximum conversion efficiency can be improved at higher values of coupled LO power using larger anodes (D0), as indicated in Fig. 5.6.(a). The question we need to answer is the feasibility of a matching network system able to fit the ideal points given in Fig. 5.6. This is because the final matching of both signals is a trade-off in order to obtain the adequate IF signal. The analyses we propose to study the stability of the matching network system consist of fixing the coupled LO power and analyzing the sensibility of the conversion efficiency to any RF impedance mismatching. The coupled LO power has been fixed at 0.8 mW and 0.4 mW in Fig. 5.8 by fixing the LO impedance required for each considered set of PSBDs. We have swept the imaginary part of the RF matching impedance while optimizing its real part to maximize the conversion efficiency of the RF into the IF signal. It is clearly possible to remark in Fig. 5.8.(a) and (b) that the diode D0 can perform the best conversion efficiency at 0.8 mW of coupled LO power, as indicated in Fig. 5.7.(a), but it is only in a very short RF impedance range. Additionally, D0 does not perform in a superior manner in any RF impedance range at 0.4 mW of coupled LO power. We can therefore conclude that D0 is probably not adequate for this frequency application. Regarding the D1 and D2 structures, we have a very interesting analysis in Fig. 5.8 since the D1 diodes perform similar or better conversion efficiencies in most of the considered RF impedance range, while D2 diodes perform the best conversion efficiency at higher RF impedance values. It is interesting to note that the real part of the RF matching impedance is very similar in both coupled LO powers. It is in accordance with the stable behavior of the real part of the RF impedance indicated in Fig. 5.7.(b) as the coupled LO power increases.

We can finally conclude that the smaller the anode size, the easier the impedance matching of the RF signal. In the case of the 600 GHz subharmonic mixer presented in section 5.1, the D1 PSBDs are the best diodes if our MMIC chip is able to match the RF signal between a real

part of its impedance from 45 Ω to 65 Ω and an imaginary part from 40 Ω to 100 Ω. However, the D2 PSBDs are better only when higher RF impedances are required to match the diode cell with the matching network of the MMIC chip. Regarding the LO impedance and the final coupled LO power, it is necessary to study the performances obtained during the ADS-HFSS optimization of the chip with diodes between D1 and D2 to finally determine the best one to cover the full required band, in accordance with the considered MMIC chip design.

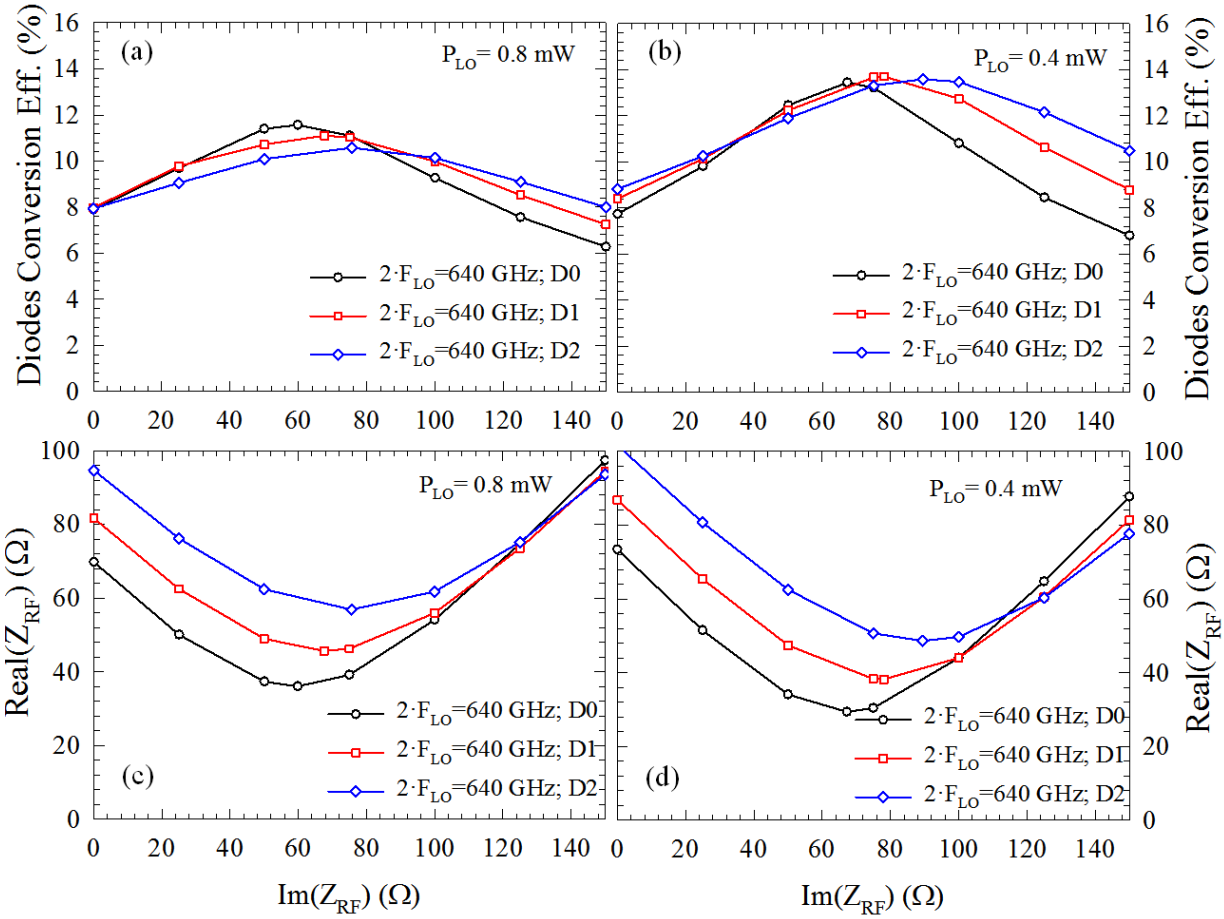

Fig. 5.8. ADS simulations of two PSBDs in antiparallel configuration for the three diodes indicated in Table V.1. It is the ideal conversion efficiency of the RF into the IF signal at (a) 0.8 mW and (b) 0.4 mW of coupled LO power when sweeping the imaginary part of the RF matching impedance. It is also plotted the ideal RF matching impedance when fixing the coupled LO power at (c) 0.8 mW and (d) 0.4 mW. The analysis has been performed at 320 GHz LO frequency. The LO impedance is fixed for each set of PSBDs.

5.3.2 Analysis of the $5\cdot10^{17}$ cm^{-3} Epilayer Doping

We extend the study to take into account another epilayer doping. The increment of the epilayer doping at $5\cdot10^{17}cm^{-3}$ has been chosen because it has been pointed out in the bibliography that the increment of the epilayer doping is adequate when increasing the frequency of mixing applications due to the reduction in the series resistance. We propose a diode D3 which features the same geometrical properties as the D1 structure used in the 600 GHz mixer, but featuring a $5\cdot10^{17}cm^{-3}$ doping of the epilayer and a slightly increased ideality factor η=1.36. The substrate effect parameters have also been modified in accordance with the increment in the epilayer doping. The considered substrate parameters are W_{EP}-W_{CA}= 21 nm and W_{CB}-W_{EP}= 9 nm. Two additional diodes are proposed to determine the suitable

modification of the geometry to reproduce the matching conditions of the LO and RF signals found in section 5.3.1. The diodes properties are indicated in Table V.2.

	Doping (cm^{-3})	W_{EP} (nm)	Area (μm^2)	I_{Sat} (pA)	η	R_S (Ω)	V_B (V)	C_{j0} (fF)
D3	$5\cdot10^{17}$	55	0.50	9.30	1.36	23.7	0.72	1.50
D4	$5\cdot10^{17}$	55	0.41	4.07	1.36	28.4	0.72	1.24
D5	$5\cdot10^{17}$	55	0.32	3.22	1.36	34.7	0.72	1.00

Table V.2. Physical and geometrical properties of the PSBDs considered in the analysis for a 600 GHz subharmonic mixer. The defined diode D3 is based on the diodes used in 600 GHz mixer presented in section 5.1 but it features an increased epilayer doping and ideality factor. The diodes D4 and D5 present a different anode size to reproduce the equivalent junction capacitance featured by diodes D1 and D2. A built-in voltage V_B= 0.72 V, η=1.36, α=0.6, W_{EP}-W_{CA}= 21 nm, W_{CB}-W_{EP}= 9 nm and β= 0.64 are considered in all cases.

The equivalent study carried out in Fig. 5.7 is completed for the new set of diodes indicated in Table V.2. The results are presented in Fig. 5.9 which have been performed at 320 GHz LO frequency when sweeping the coupled LO power in the diode cell. It is possible to observe the global increment of the conversion efficiency of the RF signal into the IF signal. At the same time, the real part of the LO and RF impedances, which maximizes the ideal performance, remains very similar to the values obtained at $3\cdot10^{17}cm^{-3}$, as we compared in next section. Additionally, the tendency of the results between the three different anodes is equivalent to the tendency observed in Fig. 5.7. This is because D4 and D5 have been defined to feature the equivalent junction capacitance featured by D1 and D2. Diodes D1 and D4 have an equivalent junction capacitance behavior but featuring a 0.1 μm^2 anode surface difference due to the different epilayer doping.

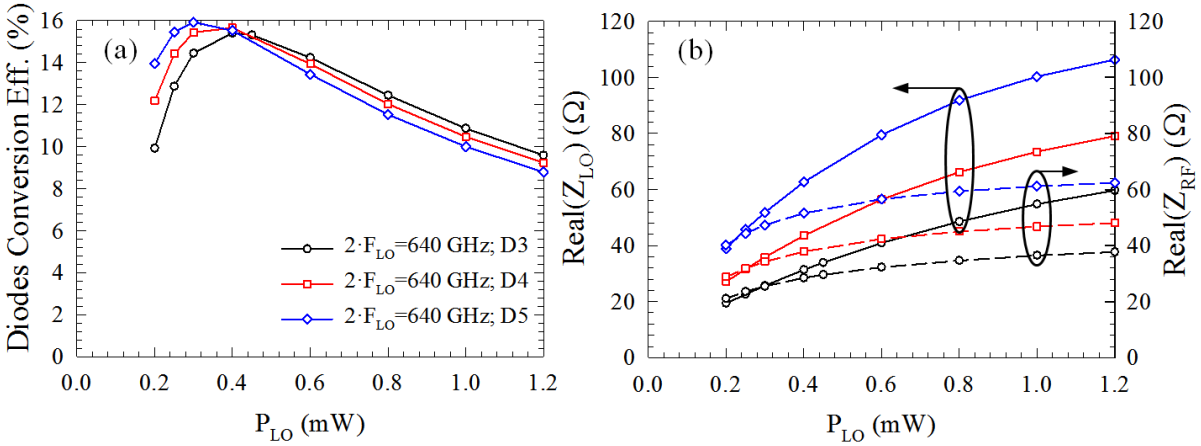

Fig. 5.9. ADS simulations of two PSBDs in antiparallel configuration for the three diodes indicated in Table V.2. It is the (a) ideal conversion efficiency of the RF into the IF signal and (b) the optimized real LO and RF impedances when sweeping the coupled LO power at 320 GHz LO frequency. The legend affects to both figures.

We have also repeated the same analysis carried out in Fig. 5.8 obtaining the same RF impedance behavior between the D1 and D4 structures as well as the D2 and D4 structures, while having sizable conversion efficiencies in all cases, as plotted in Fig. 5.10. We can obtain the same conclusions extracted from Fig. 5.7 and 5.8. Higher maximum conversion efficiency can be obtained using a larger anode in most of the coupled LO powers, as indicated in Fig. 5.9. However, it is harder to match the RF impedance of the diode cell, as

indicated in Fig. 5.10. Conversely, it is possible to have a simpler RF impedance match by using a smaller anode, as indicated in Fig. 5.10. However, the maximum conversion efficiency is reduced, as indicated in Fig. 5.9.(a). It is difficult to say which would be the final coupled LO power for each anode size in a MMIC chip design. It is therefore necessary to analyze each case while optimizing the MMIC chip. However, we can ensure the improvement of the 600 GHz mixer if the epilayer doping is increased and the anode size adequately optimized.

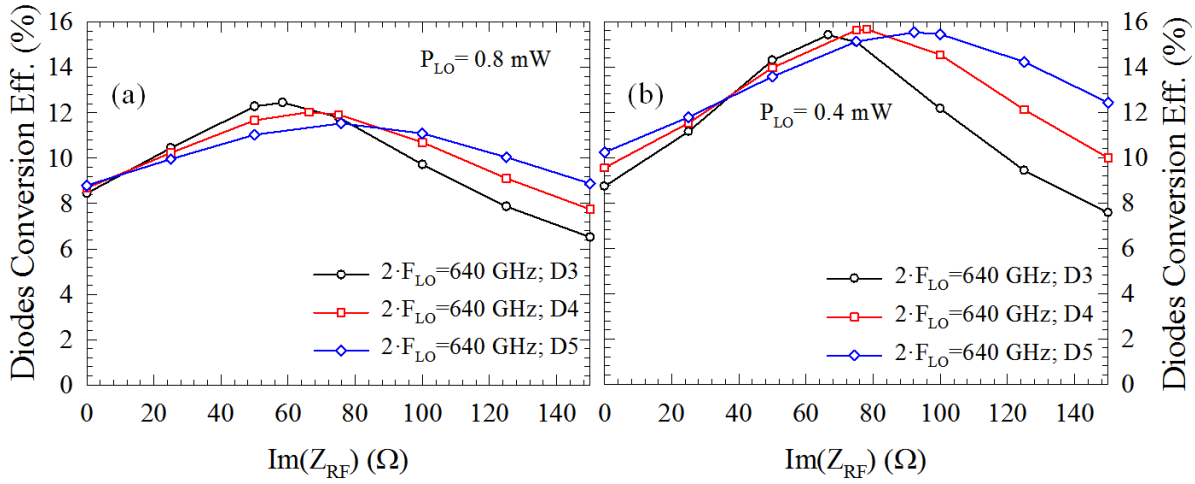

Fig. 5.10. ADS simulations of two PSBDs in antiparallel configuration for the three diodes indicated in Table V.2. It is the ideal conversion efficiency of the RF into the IF signal at (a) 0.8 mW and (b) 0.4 mW of coupled LO power when sweeping the imaginary part of the RF matching impedance. The analysis has been performed at 320 GHz LO frequency. The LO impedance is fixed for each set of PSBDs.

5.3.3 Improvement of the 600 GHz Subharmonic Mixer Performance

An improvement of the 600 GHz sub-harmonic mixer is proposed in this section in accordance with the analysis carried out in previous points of section 5.3. We first compare here the maximum conversion efficiency of the RF into the IF signal performed by D1 structure defined in Table V.1 and D4 structure defined in Table V.2. Second, we compare the RF and LO matching impedance requirements in each case in order to conclude the feasibility of a modification of the PSBDs in the already designed 600 GHz mixer.

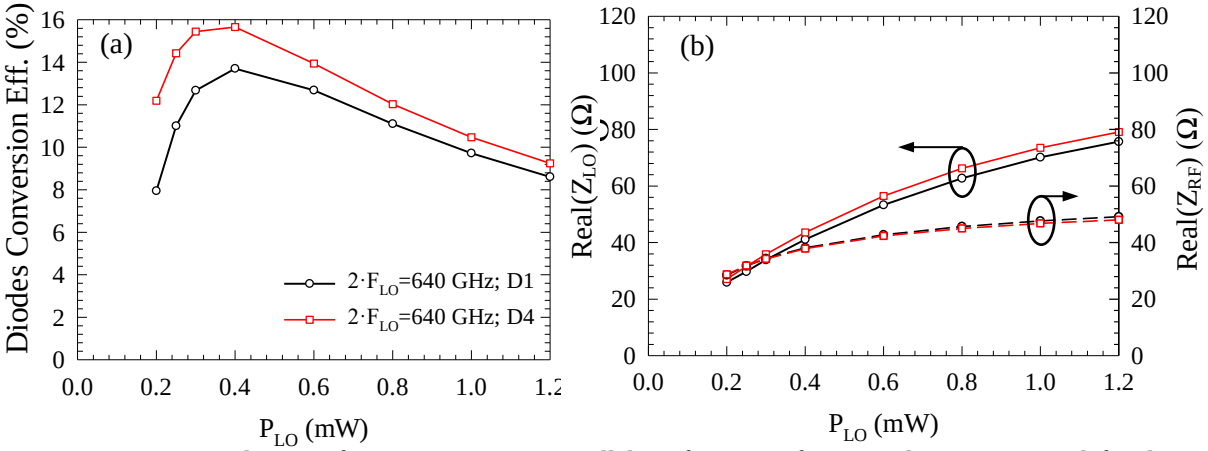

Fig. 5.11. ADS simulations of two PSBDs in antiparallel configuration for D1 and D4 structures defined in Table V.1 and 2 respectively. The (a) ideal conversion efficiency of the RF into the IF signal and (b) the optimized real LO and RF impedances when sweeping the coupled LO power at 320 GHz LO frequency. The legend affects to both figures.

The only difference between these structures is the epilayer doping, followed by a consistent modification of the physical properties of the model parameters. The anode size in the D4 structure has been adequately reduced to feature an equivalent capacitance behavior to the D1 structure. The conversion efficiency of the RF into the IF signal performed by each set of diodes in antiparallel configuration is plotted in Fig. 5.11, as well as the optimized real parts of the LO and RF signal when sweeping the coupled LO power. We can see in Fig. 5.11 the increment of the maximum conversion efficiency performed by the D4 PSBDs structure for any coupled LO power. Regarding the real part of the impedance, the real part of the RF matching impedance of the D4 structure is exactly the same necessary to match the D1 structure, while the real part of the LO matching impedance is slightly smaller in the D4 structure due to the smaller simulated resistance in the I-V curve. The question we need to answer is how the already designed MMIC chip for the D1 set of diodes can match the new D4 set of diodes. The maximum conversion efficiency and the optimal real part of the RF impedance when sweeping the imaginary part of the RF matching impedance, for 0.8 mW and 0.4 mW of coupled LO power at 320 GHz, are plotted in Fig. 5.12 to determine the new matching requirements of the RF signal.

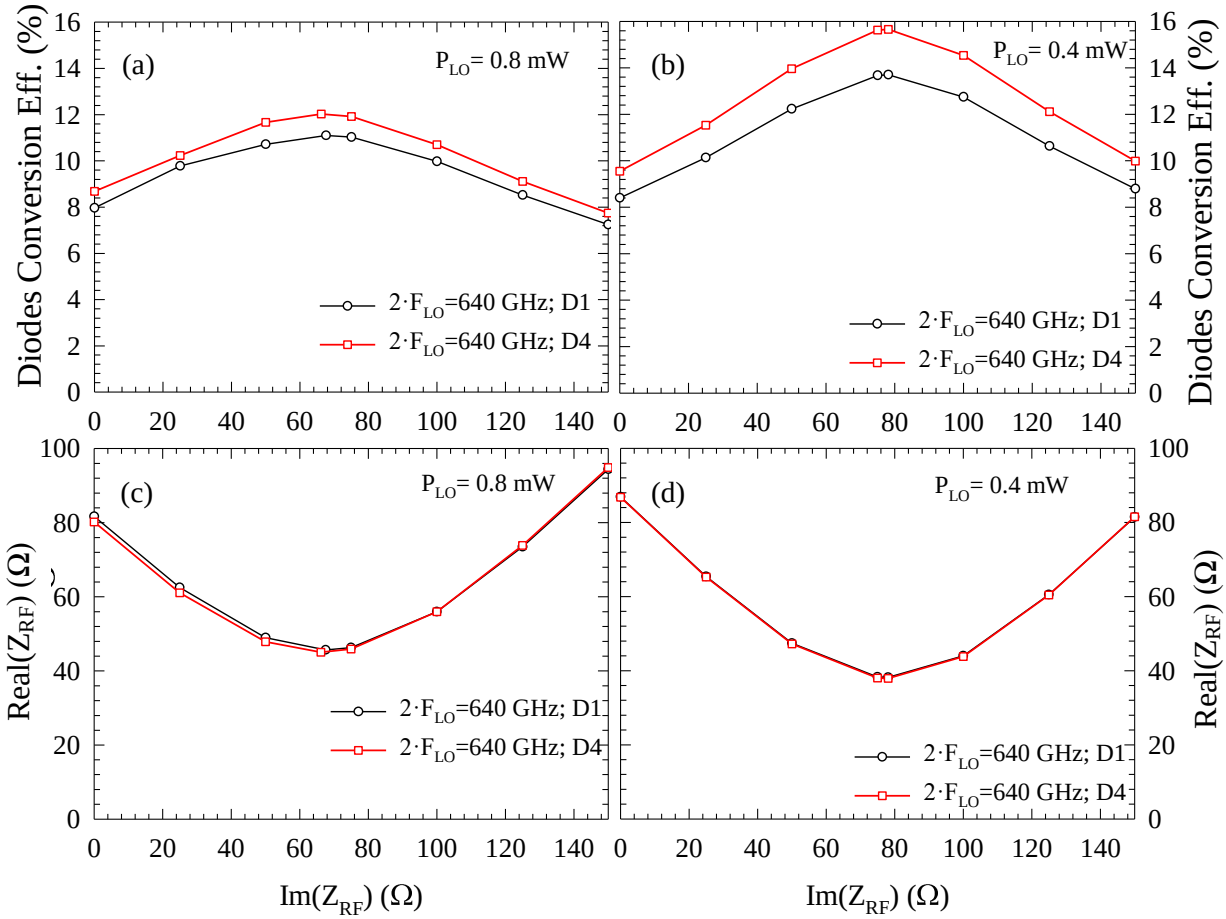

Fig. 5.12. ADS simulations of two PSBDs in antiparallel configuration for D1 and D4 structures defined in Table V.1 and 2 respectively. The ideal conversion efficiency of the RF into the IF signal at (a) 0.8 mW and (b) 0.4 mW of coupled LO power when sweeping the imaginary part of the RF matching impedance. Also plotted: the ideal RF matching impedance when fixing the coupled LO power at (c) 0.8 mW and (d) 0.4 mW. The analysis has been performed at 320 GHz LO frequency. The LO impedance is fixed for each set of PSBDs.

The conversion efficiency performed by the D1 and D4 diodes are equivalent due to the equivalent capacitance properties, but the D4 shows a better performance. It is possible to conclude, in accordance with Fig. 5.12.(c) and (d), that the RF matching network of the D1 diodes is exactly the same required for the D4 diodes. This means that the RF signal would be equivalently coupled for the D1 and D4 structures by the already designed MMIC chip of the 600 GHz mixer. The last question is related to the LO matching impedance. The D1 and D4 set of diodes have been compared in Fig. 5.13, where the real and imaginary parts of the optimal LO impedance when sweeping the coupled LO power in the diode cell, have been plotted. We can observe in Fig. 5.13 that the imaginary part of the impedance in both cases is very similar at ~0.8 mW of coupled LO power and it has a different slope in each case. At the same time, the real part of the impedance presents the same tendency in both sets of diodes and it is smaller for the D1 structure. We can conclude that the optimal coupled LO power should decrease if we use the D4 set of diodes because it is the way to recover a similar value of the optimal LO impedance matching optimized for the D1 structure. This means that the D4 set of diodes not only have a better performance, but they require a lower coupled LO power to equivalently match the designed LO matching network of the 600 GHz MMIC mixer chip.

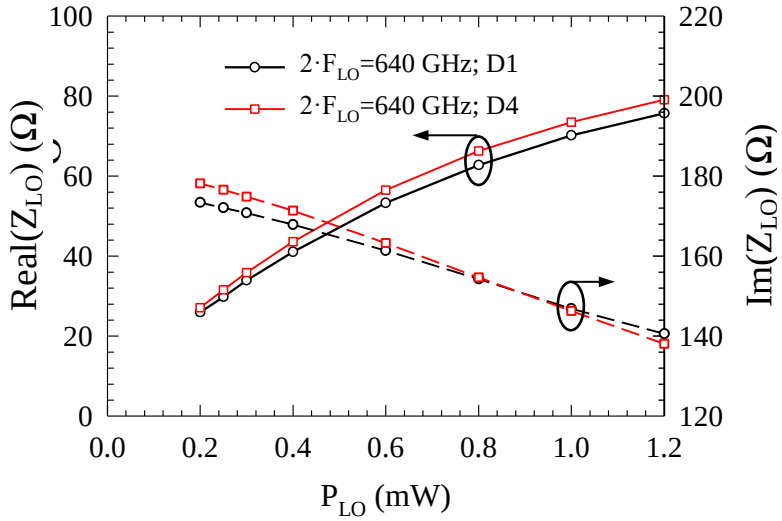

Fig. 5.13. ADS simulations of two PSBDs in antiparallel configuration for D1 and D4 structures defined in Table V.1 and 2 respectively. It is the comparison of the optimal LO impedance when sweeping the coupled LO power at 320 GHz LO frequency.

We finish this section with the implementation of the D4 PSBDs in the full ADS-HFSS test-bench described in section 5.2. We compared the conversion efficiency of the RF into the IF signal in the diode cell, when simulating a global LO input power from 1.6 mW to 2.8 mW, in the MMIC mixer chip defined in HFSS. The results are obtained in the simulated ADS-HFSS test-bench for both the D1 and D4 structures defined in Table V.1 and 2, and they have been plotted in Fig. 5.14.(a). The coupled LO power in the diode cell has been plotted in Fig. 5.14.(b) for both diodes. We can appreciate the improvement of the conversion efficiency performed by the D4 PSBD structure in Fig. 5.14.(a). We should point out that the highest conversion efficiency given by the D4 structure has been reduced from 2.8 mW to 2.4 mW of global LO input power at the high frequencies of the band. A similar reduction can be

observed at lower frequencies where 1.6 mW is enough to have the best performance of the D4 PSBDs. The impact of this reduction comes from the coupled LO power in the diode cell, which has been reduced from ~0.78 mW for the D1 PSBDs (see Fig. 5.4) to ~0.62 mW for the D4 PSBDs. This reduction was correctly predicted by the analysis presented in Fig. 5.13.

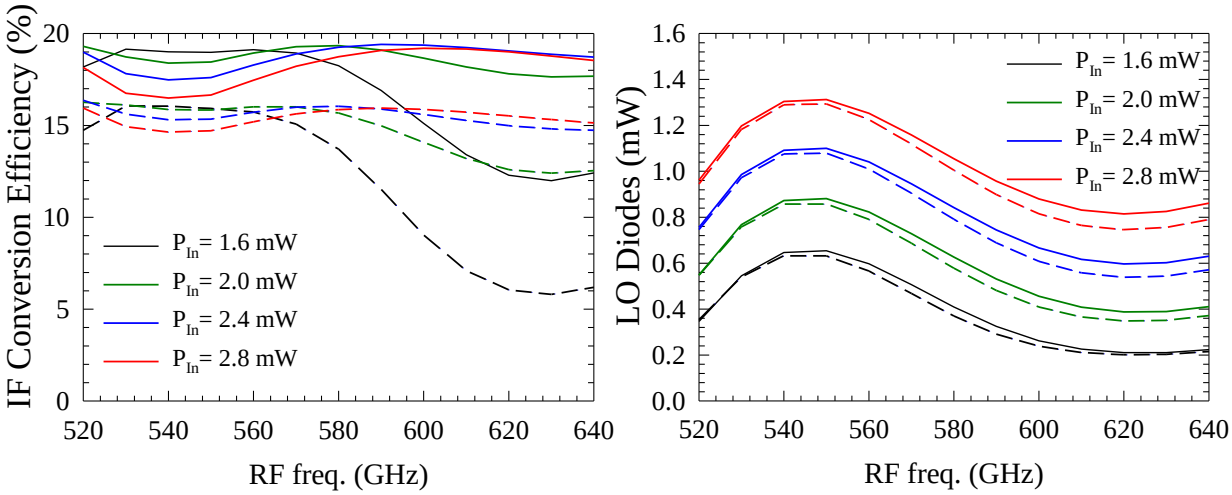

Fig. 5.14. HFSS results of the (a) conversion efficiency of the RF into the 4 GHz IF signal and (b) the LO power coupled with the diode cell when sweeping the input LO power from 1.6mW to 2.8 mW. Solid lines represent the D4 structure and dashed lines represent the D1 structure.

5.4 Conclusions

The diode cell analysis carried out in this chapter for the experimental 600 GHz mixer presented in [Treut16] has pointed out a set of properties presented by PSBDs in sub-harmonic frequency mixers featuring an antiparallel configuration of diodes (stronger and clearer). These properties are highly important when looking for the adequate set of PSBDs in a mixer design. The qualitative behavior of PSBDs can be summarized in three statements to be considered in the design of the PSBD-based mixer modules.

1- There is a specific junction capacitance range of the PSBDs able to open a frequency window in each required frequency range. The adequate junction capacitance does not depend on the PSBD epilayer properties; it only depends on the center frequency of the required bandwidth. Saturation phenomena in the electron transport are the only effect that can modify this affirmation, especially when considering low epilayer doping at very high frequencies.

2- Once the junction capacitance has been correctly determined for the considered frequency range, it is possible to define a nominal PSBD structure geometry that features this junction capacitance in accordance with the considered thickness and doping of the epilayer. The tendency of the mixer performance when considering a fixed thickness and doping of the epilayer has been studied along this chapter. On one hand, the bigger the anode size is compared with a nominal value, the higher the maximum conversion efficiency. However, it is harder to match the diode cell impedance in the optimal point as the anode increases and the bandwidth of the MMIC become sensitive to any experimental deviation from the design. On the other hand, the smaller the anode size is compared with the nominal one, the smaller the maximum conversion efficiency. However, it is easier to match the diode cell impedance in such an optimal point. That is the reason for a smaller anode size leads to a mixer design less sensitive to any fabrication defect which can introduce a deviation from the optimal point. The final anode size is a trade-off between the higher performance provided by larger anodes, the higher stability reachable by smaller anodes and the fabrication capabilities to ensure the reliability of the design.

3- If a specific value of junction capacity has already been used in a design with a specific thickness and doping of the epilayer, it is possible to have the equivalent RF matching requirements of the PSBDs for a different doping of the epilayer if the anode size is modified to reproduce a similar junction capacitance. Additionally, it has been predicted in this author that the performance is always improved when increasing the doping of the epilayer, but it requires the adequate reduction of the anode size where the only limit observed in this work is the experimental technical capabilities to reduce the anode size.

All these statements have been thoroughly considered in the design of the 1.2 THz mixer presented in chapter 6. The possible saturation phenomena are not considered in the developed model, but its influence on the device optimization is not expected to be critical due to the similar epilayer properties features by the considered set of diodes and the similar low powers managed by each PSBDs [Graj00b].

6 A 1.2 THz Sub-Harmonic Biasable Frequency Mixer

The 1.2 THz biasable frequency mixer design developed by LERMA for the SWI instrument is detailed in this chapter. It starts with the analysis of the PSBD diodes performances in section 6.1 when simulating two antiparallel diodes with the properties considered for the design. Some of the main phenomena in the mixing response of PSBDs and the impact of the simulated parameters of the diode model are discussed here. Section 6.2 is dedicated to presenting two MMIC mixer chip designs, where the main design considerations are thoroughly discussed and compared. The design of the mechanical block where the MMIC chips are mounted is presented and discussed in section 6.3. The theoretical analysis of frequency mixers, and especially the developed 1.2 THz mixers, has been carried out in section 6.4, where the conversion loss and noise temperature of the receiver are qualitatively and quantitatively discussed in terms of ADS-HFSS simulations. These concepts are then applied to the 1.2 THz mixers described in section 6.2. The first experimental results of a functional 1.2 THz receiver using the 300 GHz power-combined doubler, a 600 GHz two anodes doubler and a 1.2 THz mixer are presented in section 6.5. The experimental results are discussed in section 6.6 in terms of the individual simulations of the 1.2 THz mixer and in terms of simultaneous simulations of the 600 GHz doubler and the 1.2 THz mixer in section 6.7. The experimental results have been updated in section 6.8 with the last results obtained during the writing of this dissertation. The conclusions of this chapter are listed at the end.

6.1 Optimization of the PSBDs Properties

This section is dedicated to the analysis of the impact of the PSBDs' properties on the potential performance of the frequency subharmonic mixer at 1.2 THz. This study is based on the analysis carried out in section 5.3 for the 600 GHz subharmonic mixer. The same test bench has been defined in the ADS software and two diodes in antiparallel configuration have been simulated with ADS harmonic balance simulations using the developed SDD model. The possibility of biasing the PSBDs has been accounted for in this test bench. The PSBDs are placed in series configuration with respect to the DC power supply. The only difference is the frequency range of the LO and the RF one-tone power sources used in ADS. The IF impedance is fixed at 250 Ω to represent the IF adapter circuit. The impedance of each source is optimized to match the diode cell in the optimal point to deliver the highest IF signal into the IF port. This section is completely based on the observations obtained in section 5.3 and some considerations are accounted for in accordance with the new application at 1.2 THz. First, it was concluded in chapter 4 that the smaller the anode size of the PSBDs, the smaller the LO power required to correctly pump the diode cell (see Fig. 5.7). Second, it has also been concluded that the smaller the junction capacitance of the PSBDs, the simpler the RF coupling along the frequency band (see Fig. 5.8). Since there wasn't any problem with the LO power availability for the 600 GHz mixer presented in chapter 4, a wider set of anode sizes could be proposed for the MMIC chip optimization. However, a lack of LO power to pump the 1.2 THz mixer was expected in this application and a correct choice of the anode size of the 1.2 THz mixer PSBDs was critical. It is not because of the mixer diodes performances but it is due to the LO chain power supply. This means that the reduction of the mixer PSBDs anode size is especially important now since it allows reducing the minimum LO power required to get the optimum conversion efficiency of the diode cell. The minimum Schottky

anode size that can be fabricated by LPN to ensure the reliability of the fabrication process is ~0.2 μm^2. This analysis therefore focuses on the anode size.

Two different analyses are carried out in this section. First, the potential performances of the diode cell at different epilayer doping of the PSBDs. Second, the impact of biasing the PSBDs on the performances.

6.1.1 Analysis of the 3·10^{17} cm^{-3} Epilayer Doping

The fact of maintaining this epilayer doping is based on two important statements. First, the fabrication process of the PSBDs at this doping level is well known and successfully demonstrated in the 600 GHz mixer presented in chapter 6. Second, it allows having a lower junction capacitance of the PSBDs than at higher epilayer doping since the anode size cannot be reduced below 0.2 μm^2. The main physical and geometrical parameters of the proposed PSBDs used in the SDD model for this application are indicated in Table VI.1. The parameters indicated in Table VI.1 have been used in the developed SDD model accounting for the fringing and substrate effects explained in chapter 2, where a factor β= 0.64 is used in all simulations accounting for the surface charge influence on the PSBDs capacitance model.

	Doping (cm^{-3})	W_{EP} (nm)	Area (μm^2)	I_{Sat} (pA)	η	R_S (Ω)	V_B (V)	C_{j0} (fF)
D1	3·10^{17}	55	0.20	0.69	1.38	86.7	0.75	0.518

Table VI.1. Physical and geometrical properties of the PSBDs considered in the analysis for a 1200 GHz subharmonic mixer. A built-in voltage V_B= 0.75 V, η=1.38, α=0.6, W_{EP}-W_{CA}= 28 nm, W_{EP}+W_{CB}= 9 nm and β= 0.64 are considered in all cases.

We start analyzing the maximal conversion efficiency of the RF signal into IF signal by the diode cell, using the nominal PSBD structure D1 described in Table V.1. The maximum conversion efficiency of the diode cell when ideally coupling the LO power and optimizing the RF impedance, which maximizes the IF generation (Z_{IF}= 250 Ω) for each coupled LO power, are plotted in Fig. 6.1 for the LO frequencies 540 GHz, 590 GHz and 640 GHz.

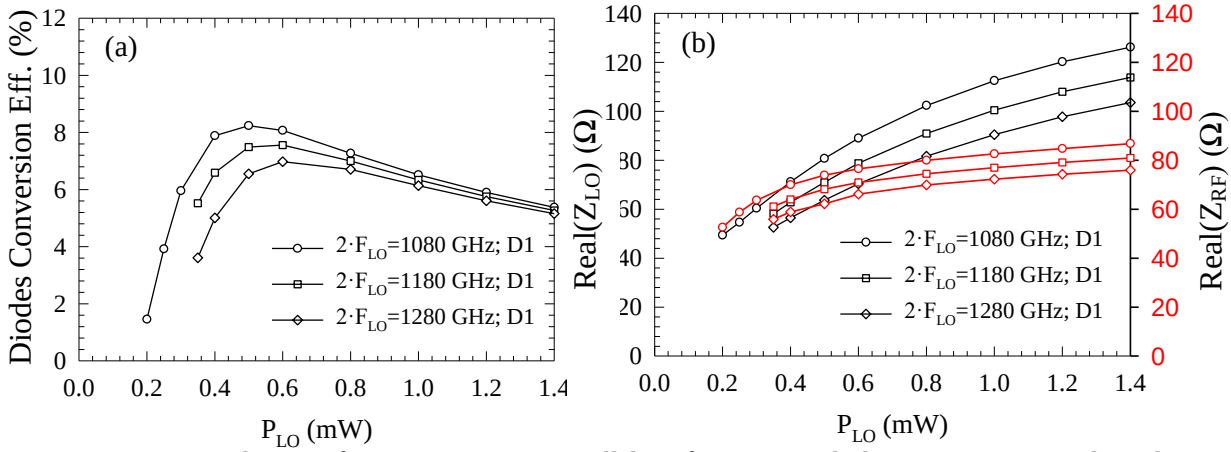

Fig. 6.1. ADS simulations of two PSBDs in antiparallel configuration with the D1 parameters indicated in Table VI.1. It is the (a) ideal conversion efficiency of the RF into the IF signal and (b) the optimized real LO and RF impedances when sweeping the coupled LO power at LO frequencies 540 GHz, 590 GHz and 640 GHz. No bias of the PSBDs has been considered

We can note that the optimal coupled LO power in the diode cell at zero bias of the PSBDs is between 0.5 - 0.6 mW along the band and the maximal conversion efficiency is reduced as the LO frequency is increased. These preliminary results reproduce exactly the same tendency previously obtained in section 5.3.1, but the minimum LO power required to be coupled in the diode cell has notably increased and the maximum conversion efficiency has notably decreased. The increment of the LO power requirements indicate that the minimum 0.2 μm^2 anode size, which is possible to fabricate by LPN, is high compared to the anode size used in the 600 GHz mixer. The 1.2 THz mixer PSBDs requires more LO power than the 600 GHz mixer PSBDs to obtain the optimal performance. If a ~50 % of LO coupling efficiency of the LO matching network is supposed for the final designed mixer, it will require more than 1.2 mW of LO input power to correctly pump the diode cell at cero mixer-bias. Regarding the optimum LO and RF impedance matching, the D1 structure of the PSBDs defined in Table VI.1 has slightly higher impedances than the PSBDs defined in section 5.3.1 for the 600 GHz mixer. This means that the matching network of the diodes needs to be more resistive and thus, the matching network losses will be higher. However, these impedance values can be obtained in practice.

It has already been demonstrated in section 4.1 that it is complicated to have more than 1 mW of LO input power to pump the 1.2 THz mixer and it was expected to be even less when the 1.2 THz mixer design started at the end of 2014. This is because the bias option is especially required for this application and it is for this reason that the author of this paper designed an improved 600 GHz four anodes doubler able to increase the LO power at these frequencies. The maximum conversion efficiency of the diode cell when ideally coupling the LO power and optimizing the RF impedance match is plotted in Fig. 6.2(a) at 640 GHz of LO frequency. This has been done to maximize the IF generation (Z_{IF}= 250 Ω) for each coupled LO power when sweeping the bias from -0.3 V to 0.3 V. The obtained optimal real parts of the LO and the RF impedances of the diode cell are also plotted in Fig. 6.2(b). The study is focused at 640 GHz of LO frequency because it is the highest frequency of the considered band for this application and it has the highest LO power requirements.

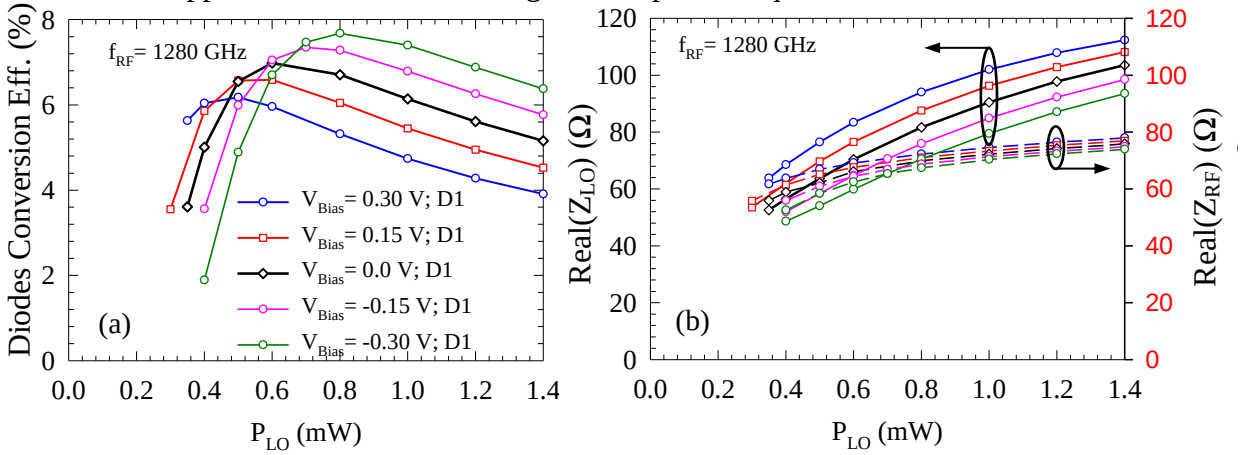

Fig. 6.2. ADS simulations of two PSBDs in antiparallel configuration with the D1 parameters indicated in Table VI.1. Ideal conversion efficiency of the RF into the IF signal (a) and the optimized real LO and RF impedances (b) when sweeping the coupled LO power at 640 GHz and different bias of the diode cell between -0.3 V to 0.3 V.

It is possible to observed in Fig. 6.2(a) the impact of the bias on the diode cell conversion efficiency. The minimum LO power required to be coupled by the diode cell can be reduced when biasing the PSBDs in inverse polarization but the maximum conversion efficiency is reduced. A better conversion efficiency of the diode cell is also predicted if the PSBDs are biased in direct polarization but a higher minimum LO power is now required. Regarding the LO and the RF coupling impedances, the optimum RF impedance is almost the same at any bias of the diode cell while the optimal LO impedance can be tuned with the diode cell bias. This means that the bias allows not only a reduction in the minimum LO power required to obtain a good performance but also to tune the LO impedance matching of the diode cell. A minimum LO input power required for this application is expected to be around 0.8 mW if a 50 % LO coupling efficiency of the mixer is supposed and a biasable chip is designed.

6.1.2 Analysis of the $5{\cdot}10^{17}$ cm^{-3} Epilayer Doping

The equivalent analysis is carried out in this section for an increased value of the epilayer doping. The main physical and geometrical parameters of the proposed PSBDs used in the SDD model for this application are exhibited in Table VI.2.

	Doping (cm^{-3})	W_{EP} (nm)	Area (μm^2)	I_{Sat} (pA)	η	R_S (Ω)	V_B (V)	C_{j0} (fF)
D2	$5{\cdot}10^{17}$	55	0.20	1.56	1.4	58.6	0.75	0.62

Table VI.2. Physical and geometrical properties of the PSBDs considered in the analysis for a 1200 GHz subharmonic mixer. A built-in voltage V_B= 0.75 V, η=1.4, α=0.6, W_{EP}-W_{CA}= 21 nm, W_{EP}+W_{CB}= 9 nm and β= 0.64 are considered in all cases.

All the observations in section 5.3 and 6.1.1 apply in this case. The maximum conversion efficiency of the diode cell when ideally coupling the LO power and optimizing the RF impedance, which maximizes the IF generation (Z_{IF}= 250 Ω), for each coupled LO power are plotted in Fig. 6.3(a) at 640 GHz of LO frequency. A bias sweep from -0.3 V to 0.3 V has been performed in this case. The obtained optimal real parts of the LO and the RF impedances of the diode cell are also plotted in Fig. 6.3(b).

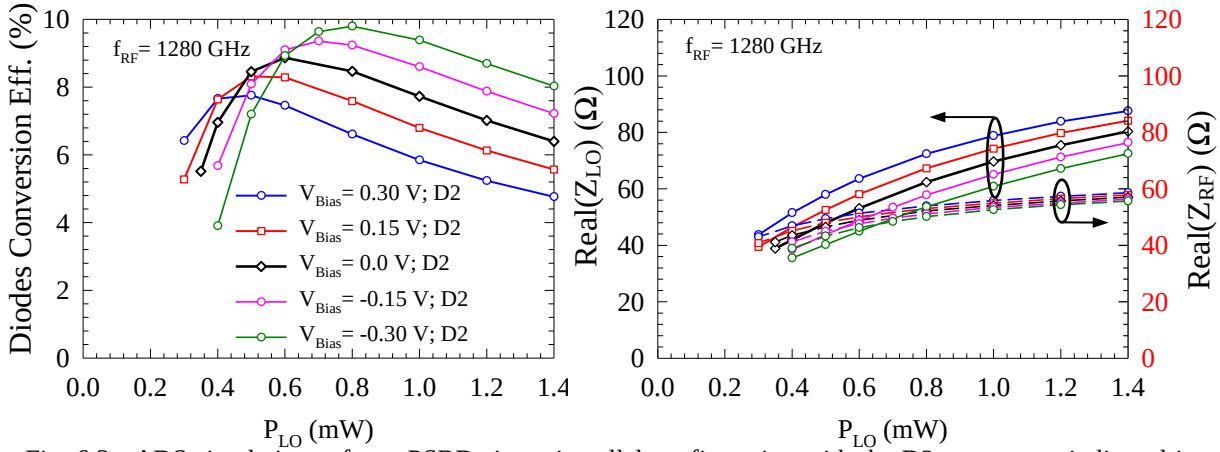

Fig. 6.3. ADS simulations of two PSBDs in antiparallel configuration with the D2 parameters indicated in Table VI.2. Ideal conversion efficiency of the RF into the IF signal (a) and the optimized real LO and RF impedances (b) when sweeping the coupled LO power at 640 GHz and different bias of the diode cell between -0.3 V to 0.3 V. The legend is applied in both figures.

It is possible to observe a higher conversion efficiency performed by the D2 structure of the PSBDs. The comparison of D1 and D2 structures for the PSBDs predicts that a ~2 % more of RF signal can be transformed into the IF signal by the D2 structure of the PSBDs and the minimum required coupled LO power does not increase in this case. The LO and the RF impedance matching of the D2 structure is lower than in the D1 structure. This improvement of the conversion efficiency has been associated with the reduced series resistance of the PSBDs since the higher junction capacitance has a negative impact at this magnitude. Regarding the LO and RF coupling, when the epilayer doping of the PSBDs is interchanged in a fixed MMIC designed chip, the same results obtained in Figs. 5.8 and 5.10 apply in this case. This means that the D2 structure is more efficient than the D1 structure but the optimal impedance matching is more constrained. However, it was already discussed in section 5.3.3 that a MMIC chip optimized for a specific epilayer doping of the PSBDs is capable of coupling a lower LO power if the epilayer doping is increased due to the lower LO impedance matching with an equivalent RF impedance. This means that the optimal LO coupled power in an MMIC chip, optimized for the D1 set of PSBDs, remains efficiently coupled if the epilayer doping is slightly increased, identical to the D2 set of PSBDs. The only negative impact can be found at high frequencies of the band due to the increment of the junction capacitance. This study will be applied in section 6.7 to demonstrate the improvement in the already designed 1.2 THz mixer.

6.2 Description of two Different 1.2 THz Mixer Chip Designs

This section is dedicated to the precise description of two different designs proposed by LERMA for the 1.2 THz sub-harmonic biasable mixer. The final designs are first presented to point out the main differences between each of them. The special considerations required in the LO and RF matching network for each one during the design and optimization are discussed next. The full design has been inspired by the already functional 600 GHz mixer presented in [Treut16].

6.2.1 In-channel and Out-channel Designs of the Chip

Two different designs have been developed by LERMA for the 1.2 THz sub-harmonic biasable mixer in this section. The properties of the PSBDs and most of dimensions of the matching network are the same in both designs, where the main difference is the positions of the diode cell with respect the LO and the RF signals matching network. The so-called "in-channel" design is shown in Fig. 6.4 and it presents the diode cell inside the middle channel defined between the LO and the RF input signals in the MMIC chip, while the "out-channel" design, shown in Fig. 6.5, has the diode cell out of the middle channel and it is placed in one side of the MMIC. The out-channel design presented in Fig. 6.5 uses the same parts but the diode cell has been placed in one side of the MMIC chip and the rest of the structures have been consequently re-optimized. It is important to state that the in-channel design was developed by the author of this manuscript during the optimization of the out-channel design in direct collaboration with Dr. A. Maestrini.

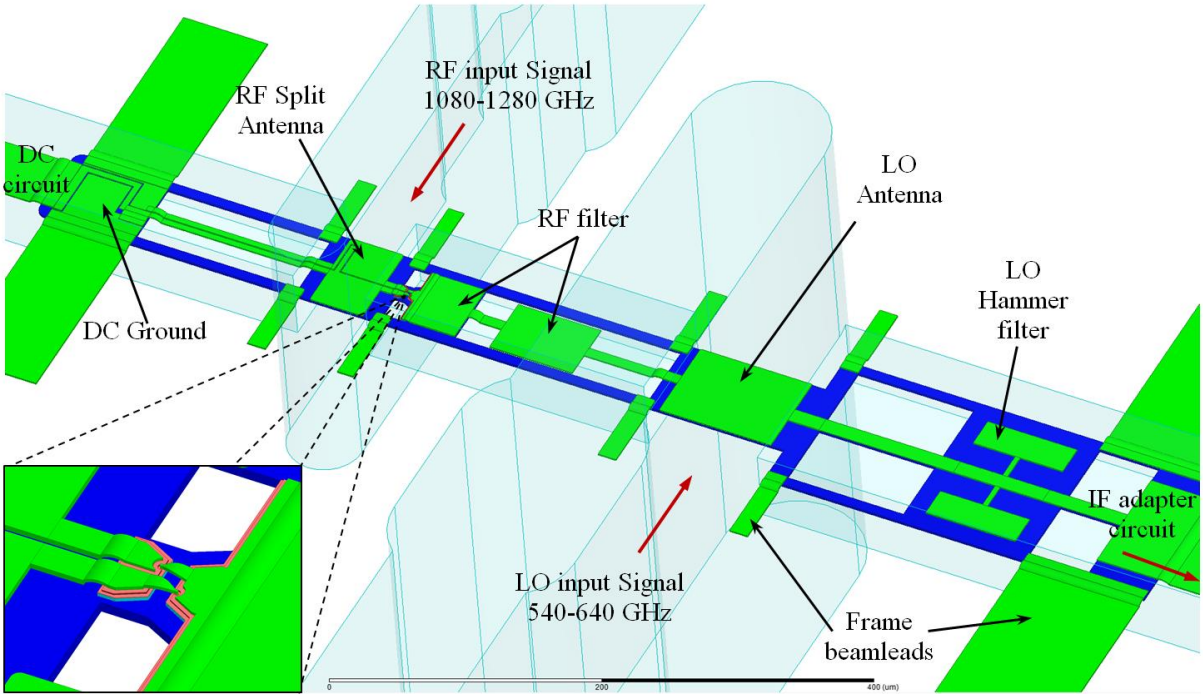

Fig. 6.4. The 1.2 THz sub-harmonic biasable HFSS chip of the in-channel design. The antiparallel diodes configuration has been specifically noted.

Regarding the similarities between both designs, the same thickness and width of the membrane has been used. Equivalent dimensions of the waveguides are used for the RF, LO and the middle channel. The IF and DC circuits are equally separated at each side of the

MMIC chip and both consist of an LO antenna that is able to correctly capture the incoming LO signal in the considered frequency range. The LO hammer filter prevents the LO signal from being lost in the IF circuit. The RF antenna is able to correctly capture the incoming RF signal in the considered frequency range and the RF filter avoids the RF signal from being lost in the IF circuit. A DC ground is used to generate the virtual ground for the RF and LO signals while it defines the DC path for biasing the PSBDs in series configuration. The IF adapter and the DC circuits are separately placed in both designs in order to simplify the DC circuit design, reduce the length of the split lines, and obtain additional freedom to design the mechanical block. The diode cell and the DC ground structures present an on-chip capacitor to correctly generate the DC path to bias the diodes in series configuration. This will be detailed in next sections.

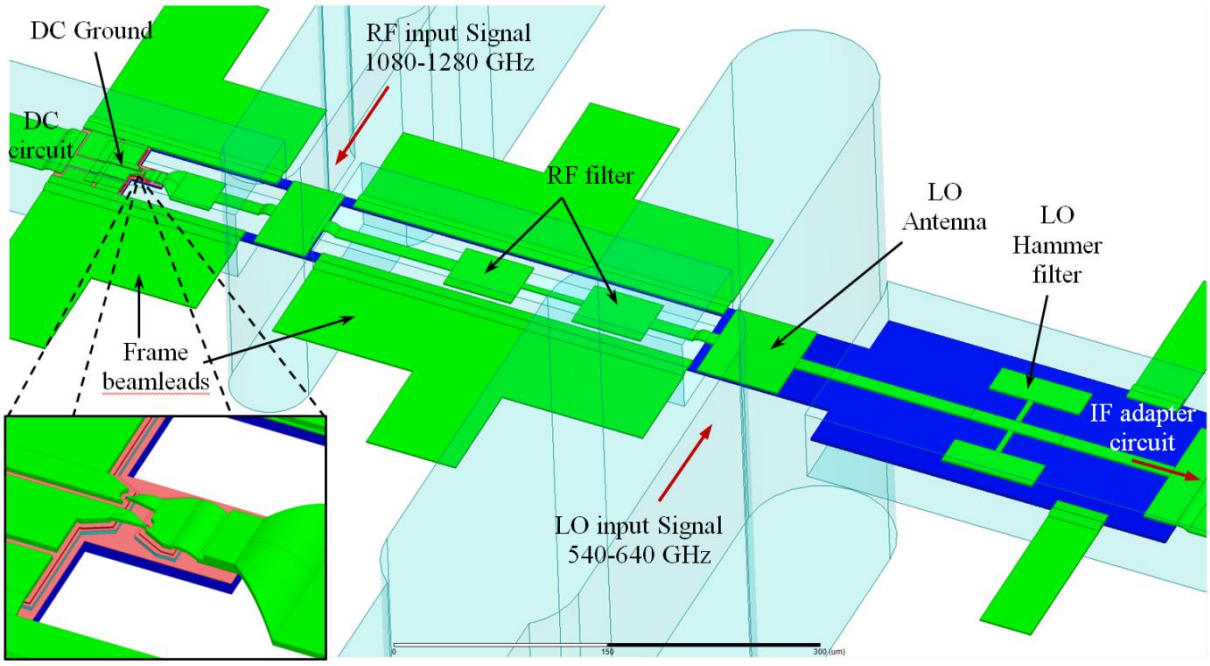

Fig. 6.5. The 1.2 THz sub-harmonic biasable HFSS chip of the out-channel design. The antiparallel diodes configuration has been specifically noted.

The main differences between the in-channel and the out-channel designs, presented respectively in Fig. 6.4 and 6.5, is the way the DC path is defined in each design in addition to the middle channel length used for the RF filtering. First, the split line and RF antenna are required for the in-channel design while it is not required for the out-channel design. Second, additional space in the middle channel is achieved in the out-channel design that enables a better optimization of the RF filter sections. The presence of a split line and RF antenna in the in-channel design is translated into additional transmission losses associated with the additional TEM mode that propagates in the split line. Regarding the frame beamleads, different distributions are proposed in each design but it does not have any other usefulness other than placing the chip on the mechanical block and defining the virtual ground. The next sub-sections of this section are dedicated to discussing each part of both designs, paying special attention to the optimization peculiarities found during the design process of each chip.

6.2.2 LO antenna and Hammer Filter

The LO and the hammer filter are the most similar parts used in both designs since no special modifications have been required when changing the diode cell position in the chip. The LO section for each design is shown in Fig. 6.6, where the images have been correctly dimensioned to appreciate the real proportions between each design. The reduction of the membrane for the in-channel design has been proposed to reduce the LO transmission losses, since the LO signal enters from the LO antenna and propagates to the hammer filter where it is reflected and propagated toward the diode cell section. The width of the LO filter channel is larger than the middle channel width in order to have a more efficient LO filter in the considered frequency range. An additional propagation mode of the RF signal exists in this section due to the increment of its width $a_{LO;Hammer}$, but it has no impact in the performances since most of the RF signal does not reach this section of the chip.

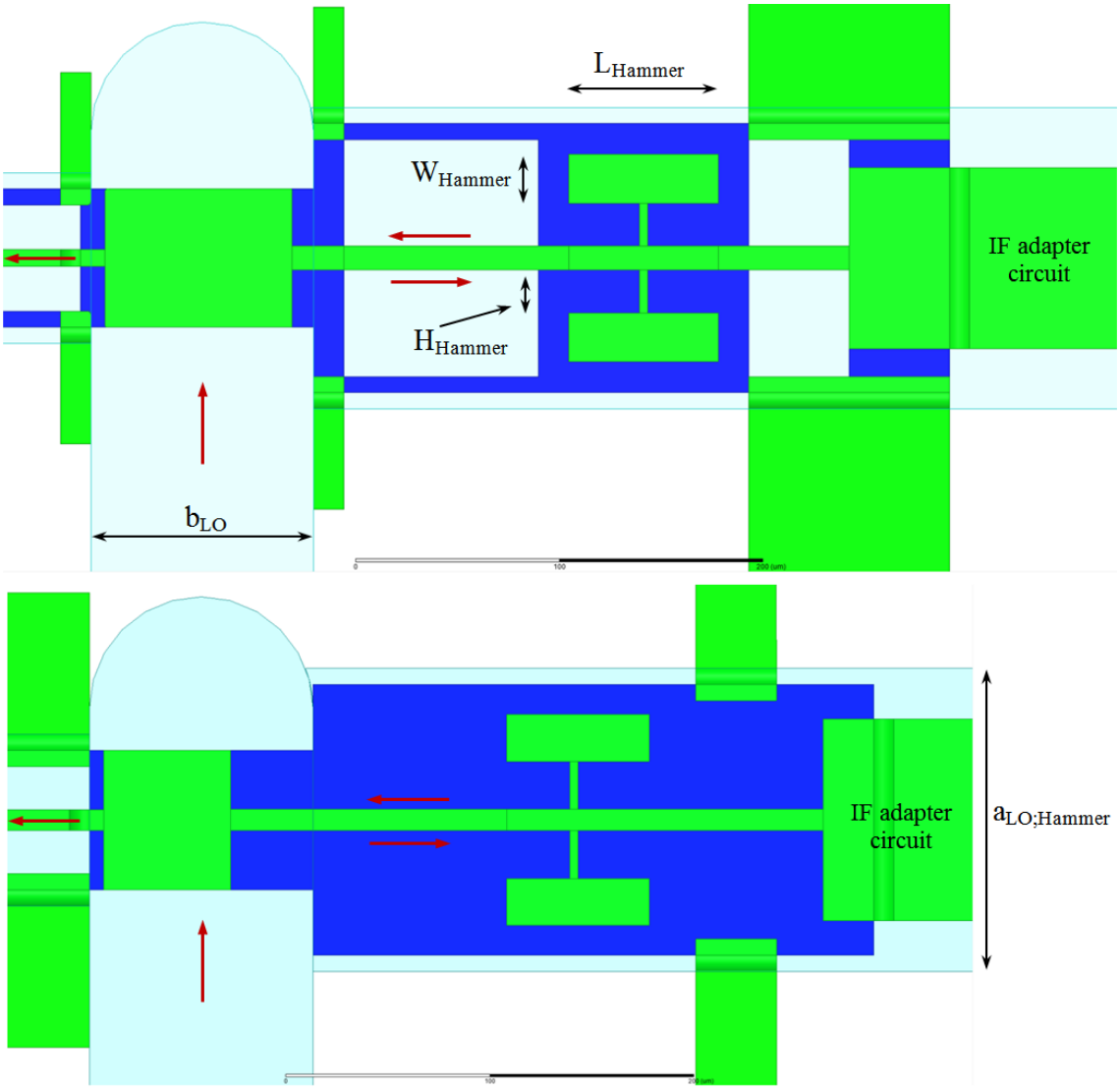

Fig. 6.6. The 1.2 THz sub-harmonic biasable HFSS chip of the (a) in-channel and (b) out-channel LO antenna and filter design. Both images have been represented with the same scale. Red arrows indicate the main LO signal propagation.

The hammer filter was designed using a HFSS optimization tool where the L_{Hammer}, W_{Hammer} and the H_{Hammer} were optimized to reduce as much as possible the transmission of the LO

signal from the LO antenna to the IF adapter circuit. This kind of filter has proven to be much more efficient than the rectangular filters, used in the 300 GHz doubler presented in section 4.1, while they are also more compact. It performs a -45 dB propagation factor of the LO signal around 600 GHz, lower than -30 dB in most of the band and lower than -20 dB in the full considered frequency band. The larger LO antenna used for the in-channel design is associated with the LO matching network of the diode cell with the increment of the antenna needed to cover the required bandwidth. A smaller LO antenna was required in the out-channel design due to the reduced constrains in the middle channel for the LO matching with the diodes. A slightly extended membrane under the LO antenna is proposed in the in-channel design, where the membrane enters 5 μm in the middle channel. This additional membrane can reduce any possible coupling resonance of the LO signal in the antenna and slightly reduce the impact of any misalignment during the placement of the fabricated chip on the mechanical block.

6.2.3 DC Ground Structure

The DC ground structure for each design is shown in Fig. 6.7. The ground design is modified in each design due to the position of the diode cell. The ground structure is usually dedicated to generate the virtual ground for the RF and LO signal where both signals should be reflected as much as possible. However, the ground structure needs to be modified in both designs to allow the definition of the DC path that will bias the diodes in series configuration. Regarding the in-channel design, the aim of this structure is correctly get the LO and RF signals grounded to reflect as well as possible any incoming signal towards the diode cell placed in the middle channel. Two elements have been required to correctly design this section of the chip. First, a split transmission line section is defined, thus an additional TEM propagation mode needs to be accounted for during the virtual design. The normal quasi-TEM mode is generated between the transmission line section and the walls of the channel that surrounds the chip and the additional TEM mode is generated between the two lines of the split transmission line. Second, an on-chip capacitor is required to define a ground path for the RF and the LO signals while it prevents the line of the split transmission line connected to the DC circuit to be grounded. The asymmetric profile of the split line in the ground section was found useful to also reflect the second TEM propagation mode of the split line. The on-chip capacitor was designed as small as possible while the LO and RF signals are correctly grounded. The length of the ground section was designed as small as possible to ensure a good ground. The split line section is substrateless to reduce the RF and LO losses. The aim of this ground section becomes much more complex in the out-channel design since the diode cell is placed in this section of the chip. The use of split transmission lines for the DC path definition is strongly reduced in this design, since there is not any split section where the RF and LO signals are propagated, but the geometry of the split ground structure plays a main role to correctly get these signals grounded. The RF and LO signals are expected to come from the middle channel, thus transmission line sections 1 and 2 are dedicated to correctly match the diode cell with the reflected RF and LO signals in the ground section place on the back of the diode cell. The reduction of the distance between the diode cell and the ground structure was found to be necessary during the optimization process, and the diode cell was therefore integrated in the DC ground structure design. Full HFSS simulations are required to

correctly account for the interaction between the diodes and the reflected RF and LO signal in the ground structure.

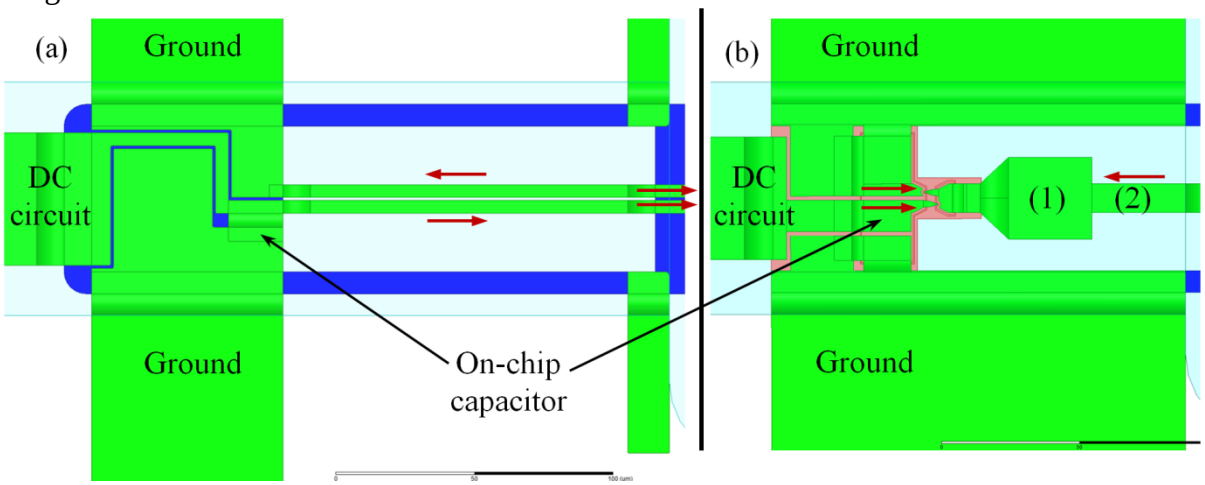

Fig. 6.7. The 1.2 THz sub-harmonic biasable HFSS chip of the (a) in-channel and (b) out-channel DC ground structure. The diode cell is placed in this section of the out-channel design. Both images have been represented with the same scale. Red arrows indicate the main LO and RF signals propagation.

Additionally, the final length of the ground section depends on the way the RF and LO signals are reflected to match the diode cell with the incoming signals from the middle channel. The on-chip capacitor used in the out-channel design of the 1.2 THz mixer has been shown in Fig. 6.8, where the transmission lines connected with the ohmic and Schottky contacts of each diode have been erased. The on-chip capacitor isolates the Schottky contact of one diode from the ohmic contact of the other antiparallel diode. The DC circuit is therefore prevented from being grounded by the frame-beamleads. This on-chip capacitor defines a series DC path configuration of the diodes.

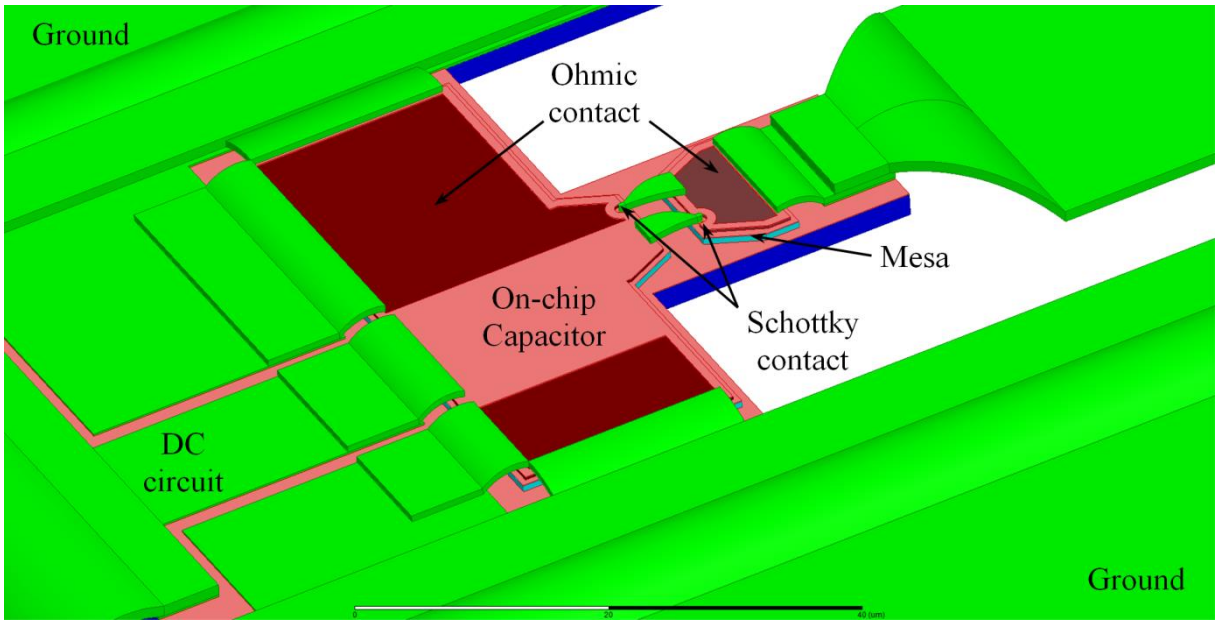

Fig. 6.8. The 1.2 THz sub-harmonic biasable HFSS chip of the out-channel design, where the on-chip diode cell design have been remarked. The transmission lines connected with the ohmic and Schottky contacts of each diode have been erased to show the on-chip capacitor design.

The equivalent concept is applied in Fig. 6.7.(a) for the in-channel design to generate the DC path for the diodes. However, another on-chip capacitor in the diode cell, a split transmission

line, and a RF split antenna are required due to the separated definition of the DC ground structure.

6.2.4 RF Filter and Antenna

The RF horn and filter sections for each design are shown in Fig. 6.9. The RF filter and antenna are modified in each design due to the position of the diode cell. The out-channel design presents a very simple geometry of the RF antenna which is dedicated to capture the RF signal in the considered frequency range. There is membrane under the RF antenna while the RF filter in the middle of the channel is substrateless to reduce the RF and LO transmission losses. The RF filter is based on rectangular filtering and it is very effective due to the absence of the diode cell which allows a much better optimization of the RF filtering. The objective of the out-channel design is to have most of the RF signal leading toward the left side of the chip where the diode cell is placed. Both the LO and the RF signals must converge on the diode cell in the correct way to have a standing wave coupling the diodes at that specific point of the chip. Hammer filters were tried for the design of the out-channel chip but their optimization is very complex and they introduce too much LO signal loss. The RF signal is filtered/reflected by the different transmission lines sections due to its lengths and the different impedances associated to each section width. The length of the sections dedicated to block the RF transmission are around $\lambda_{RF}/4$, since the wavelength of the RF signal propagated in a transmission line is $\lambda_{RF}/2$. The RF signal that arrives into a rectangular filtering section is partially transmitted and reflected, in accordance with the impedance presented by each section. It is possible to annihilate the incoming signal, with the reflected signal, if the length of the transmission line section is around $\lambda_{RF}/4$. The higher the impedance difference between two sections, the higher the reflected signal in that transition. The combination of the impedance difference and the sections lengths blocks the RF transmission toward the IF adapter circuit. Transmission line sections 2, 3 and 4 in the out-channel design are dedicated to adequately reflect the RF signal in the full frequency band. The transmission line section 5 leads the interaction between the incoming LO signal from the LO antenna and any reflected LO signal by the RF filter in the middle channel. It is desirable to reduce its length as much as possible. The transmission line section 1 is linked with the transmission line sections of the DC ground structure and its optimal length is a trade-off between the coupled LO and RF signals with the diode cell placed in the DC ground structure, i.e., the length of the transmission line section 1, in Fig. 6.9.(b), linked with the transmission line sections 1 and 2 in Fig. 6.7.(b) allows to control the electrical path of the LO and RF signal to get the diodes in the correct way to match them.

Regarding the in-channel design, the presence of the diode cell in the middle channel leads to a very different matching network design. First, the RF antenna is modified to generate the DC path required to bias the diodes in series configuration. This has been accomplished by using a split antenna where an additional TEM propagation mode appears and needs to be accounted for. The diode cell has been placed as close as possible to the RF antenna and the membrane under the RF antenna has been extended 5 μm inside each side of the channel. The extended membrane under the RF antenna allows eliminating a resonance generated in the antenna due to the split sections. The asymmetric profile of the split RF antenna was found

necessary to break the symmetry that allowed the second TEM mode of the antenna to be excited by the incoming RF signal in the waveguide and it was placed in the opposite side of the back-short of the waveguide to minimize any interaction between them. In addition, the aim of this design is having a convergence of the RF and LO signals in the diode cell, i.e., it is required to generate an RF standing wave on the diode cell between the RF signal filtered/reflected by the RF filter, defined in the middle channel, and the RF signal reflected in the DC ground structure placed in the left side of the chip. This results in a very constrained optimization of the RF filter in the middle of the channel, since it has to filter/reflect the incoming RF signal while it couples the diode cell with the reflected RF signal from the DC ground.

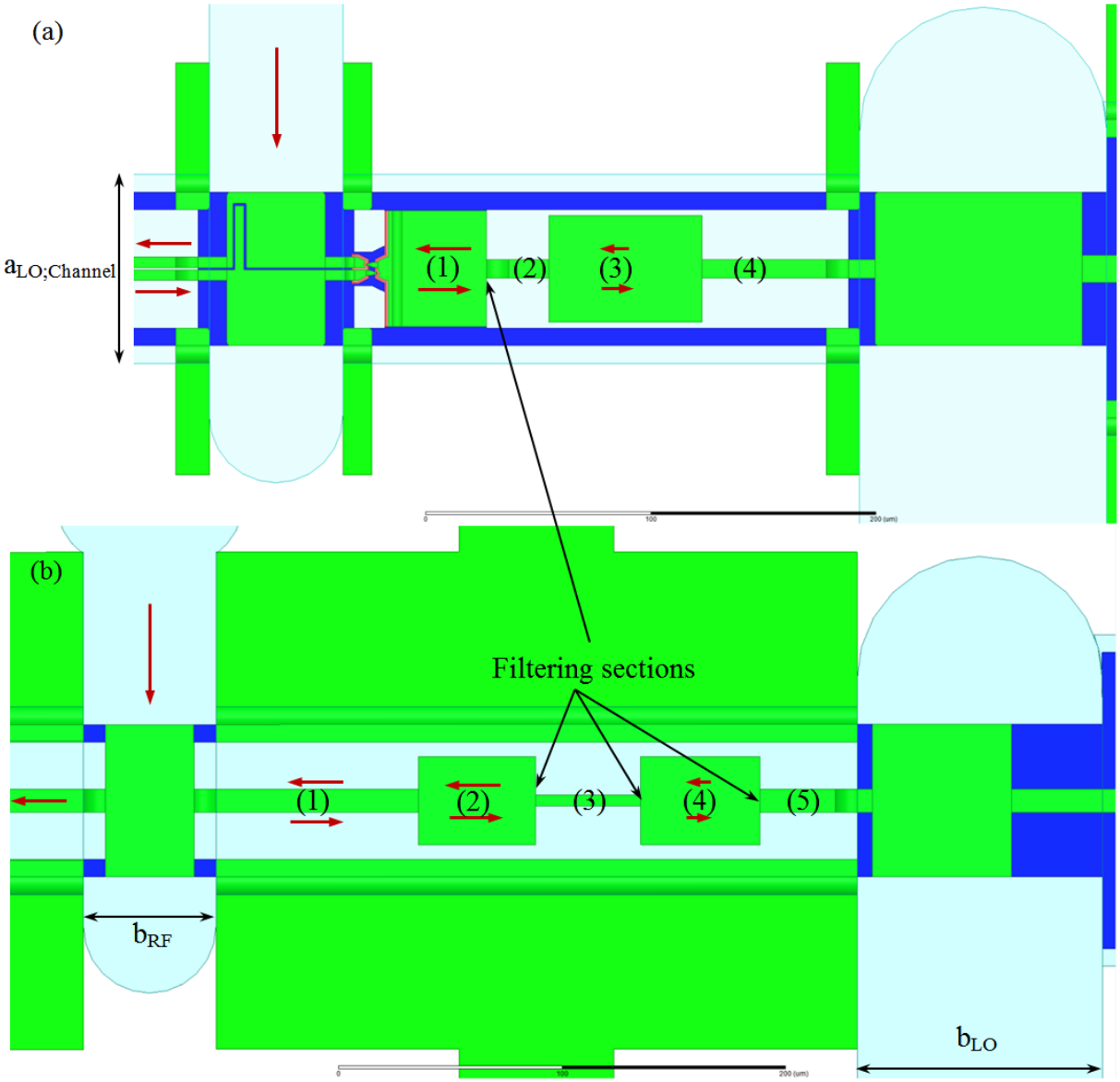

Fig. 6.9. The 1.2 THz sub-harmonic biasable HFSS chip of the (a) in-channel and (b) out-channel RF antenna and filter design. The diode cell is placed in this section of the in-channel design. Both images have been represented with the same scale. Red arrows indicate the main LO signal propagation.

Equivalently, the LO signal has to cross the middle channel, being reflected in the DC ground structure and generating a standing wave with the incoming LO signal on the diode cell. This results in a complex optimization of the middle channel structure in this design

where it is possible to appreciate that only the section 1 has a length around $\lambda_{RF}/4$ and it was adequate to be placed as closed as possible of the diode cell. The rest of transitions have the objective of both reflecting as much RF signal as possible and matching the generated standing waves of the LO and RF signals with the diode cell. A successful matching network of the RF and LO signals is led by the split transmission line of the DC ground section in Fig. 6.7.(a), which defines the adequate electrical path of the LO and RF signals to correctly match the generated standing waves with the diode cell. The transmission line section 1 of the in-channel design has a membrane under the transmission line while the sections 2, 3 and 4 are substrateless to reduce the RF and LO transmission losses. Several alternatives were accounted for in the middle channel structure design but the final one presented in Fig. 6.9.(a) was the most efficient one.

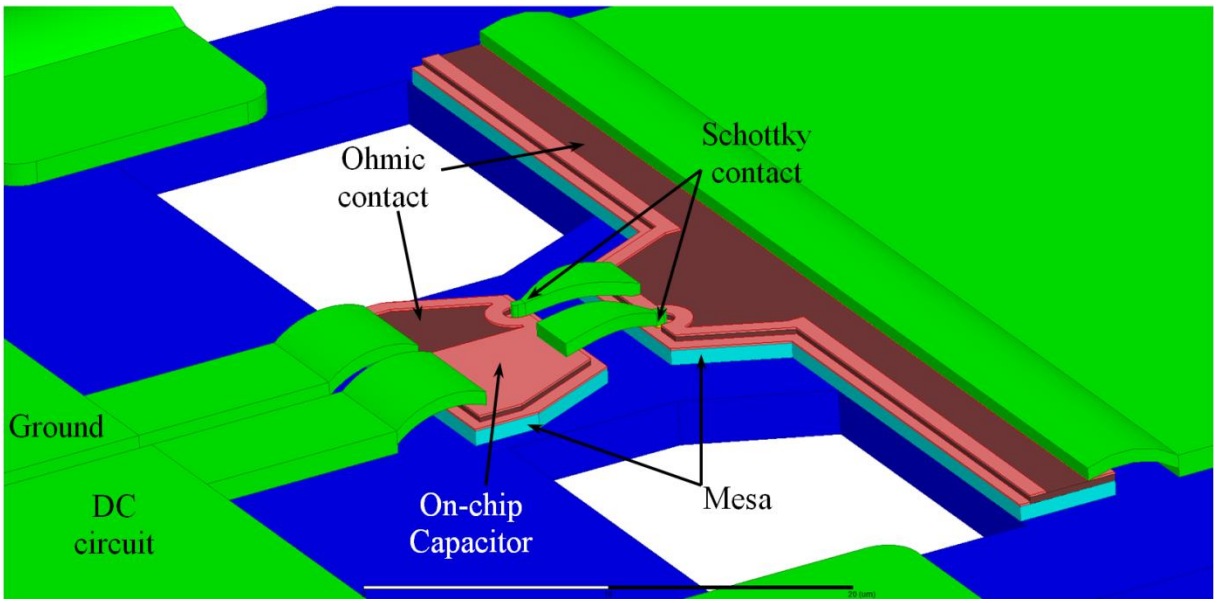

Fig. 6.10. The 1.2 THz sub-harmonic biasable HFSS chip of the in-channel design, where the on-chip diode cell design has been noted. The transmission lines connected with the ohmic and Schottky contacts of each diode have been erased to show the on-chip capacitor design.

The on-chip capacitor used in the in-channel design of the 1.2 THz mixer are shown in Fig. 6.10, where the transmission lines connected with the ohmic and Schottky contacts of each diode have been erased. The on-chip capacitor isolates the Schottky contact of one diode from the ohmic contact of the other antiparallel diode and the DC circuit is prevented from being grounded in the DC ground structure as discussed in Fig. 6.7.(a). The on-chip capacitor defines a series DC path configuration of the diodes.

6.3 Mechanical Block: IF and DC Circuits

This section is dedicated to the design of the mechanical block where the MMIC chips of the fabricated 1.2 THz mixer will be placed. The mechanical block of 1.2 THz mixer must correctly align both the RF antenna and the 600 GHz doubler presented in chapter 7. Additionally, it must define a DC connector to bias the diodes while blocking the IF signal and an IF connector to extract the IF signal. The most critical points in the design of the 1.2 THz mixer block are the high transmission losses of the RF and LO signals at these high frequencies, together with the low available LO power, and the correct filtering of the IF signal in the dc circuit. The design of the mechanical block for the 1.2 THz mixer chips shown in Fig. 6.5 is presented in Fig. 6.11, where it is possible to observe the different parts of the block and the reduced transmission path of the LO and RF signals to reduce the transmission losses. The DC circuit consists of a series of non-grounded capacities which are bounded to each other to lead the DC bias from the DC connector to the diodes. One of the capacities is grounded in this circuit (indicated in the figure) since the IF signal generated in the diode cell has a direct path to the DC circuit due to the on-chip capacitor discussed in Fig. 6.8.

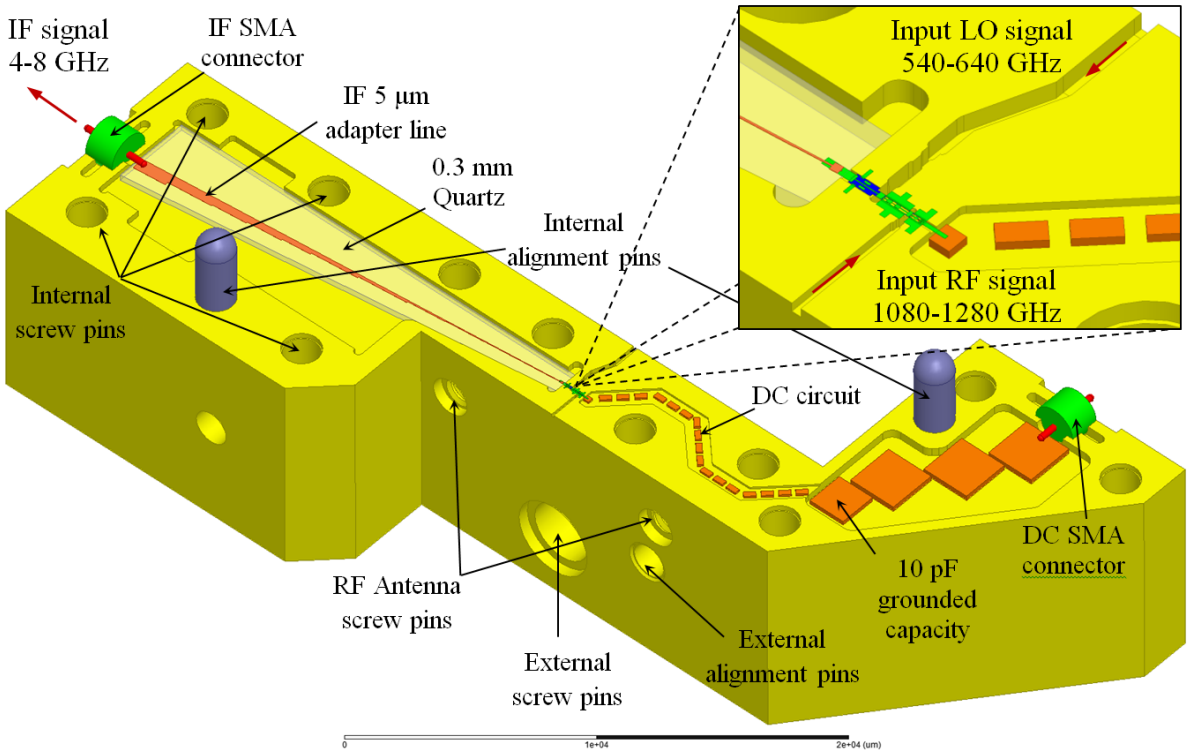

Fig. 6.11. The mechanical block of the 1.2 THz sub-harmonic biasable mixer chips. The different elements and parts of the block have been indicated. The structure in the proximities of the MMIC chip has been specifically noted. A 5 mm thickness block has been defined between the LO and RF input signals. The block is 4.5 cm length and 1.91 cm width without considering the SMA connectors.

The MMIC chip is pumped with the LO signal generated by the 600 GHz doubler discussed in chapter 3 while the RF signal comes from the RF antenna (non-plotted in Fig. 6.11). The thickness of the block between the 600 GHz doubler and the RF antenna has been reduced down to 5 mm, with ~3.5 mm of these corresponding to the LO path and ~1.5 mm to the RF path. The IF circuit is a 2.1-cm-length impedance adapter in a longitudinal distribution. The

longitudinal geometry simplifies the virtual design with respect the IF circuit presented in Fig. 5.1.1. However, it is also expected to suffer stronger deformations associated to temperature variations. The IF adapter transmission line consists of a 5-µm-thick gold transmission line on a 300-µm-quartz substrate that adapts the 250 Ω impedance of the input IF signal with the nominal 50 Ω impedance of the SMA connector. The resulting IF adapter circuit presented in Fig. 6.11 has been optimized to maximize the IF transmission between the MMIC chip and the DC connector. The resulting IF signal is then led to the low noise amplifier (LNA) for data treatment.

6.3.1 IF Circuit

Little discussion has been devoted to the IF adapter circuit. The IF adapter circuit is detailed in this subsection and the main considerations in the design are discussed. The presented IF adapter circuit design presented in Fig. 6.11 was carried out by LERMAs microwave engineer Frédéric Dauplay using the 3D Electromagnetic simulator software "Computer Simulation Technology" (CST). The main IF adapter circuit proposed for the 1.2 THz mixer and designed in CST is presented in Fig. 6.12. This circuit consists of a 5-µm-thick gold transmission line on a 300-µm-quartz substrate, electrical relative permittivity ε_r=3.78, that adapts the 250 Ω impedance of the input IF signal with the nominal 50 Ω impedance of the SMA connector. A conductivity σ= $2 \cdot 10^7$ S/m has been simulated in the gold transmission line and the walls of the IF cavity. The simulation of the real dimensions of the IF cavity defined in the mechanical block, the quartz substrate, the transmission line and the SMA connector need to be simulated to correctly account for the interaction of the IF propagation mode in the adapter circuit.

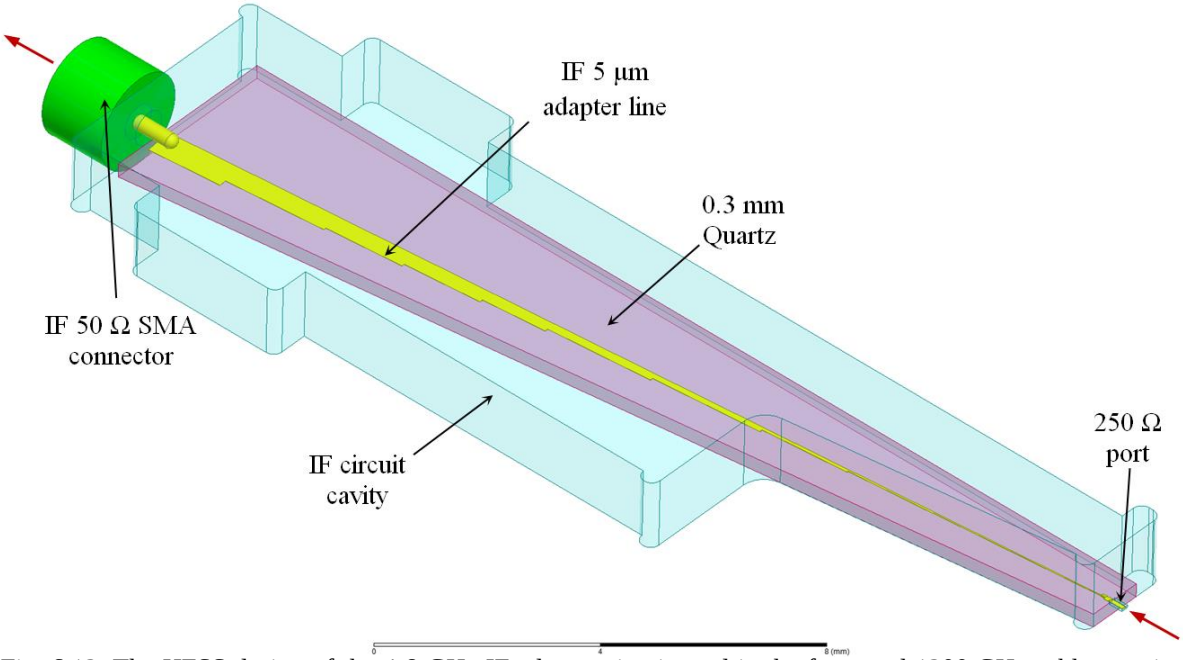

Fig. 6.12. The HFSS design of the 4-8 GHz IF adapter circuit used in the front-end 1200 GHz subharmonic frequency mixer. It has been optimized to adapt a 250 Ω IF impedance in port one with the 50 Ω impedance of the SMA connector in port 2.

The length of the different steps of the transmission line are then optimized to maximize the IF transmission between the MMIC chip and the connector in the considered bandwidth from

4 to 8 GHz. It is important to mention that the 250 Ω and 50 Ω in each side of the IF adapter must be imposed in the simulated ports during the electromagnetic simulations since 250 Ω is not the intrinsic impedance of the chip section connected to the IF circuit. We recall that the external IF impedance at 250 Ω was used during the optimization of the MMIC chips in ADS-HFSS simulations, indicated in Fig. 6.3 and 6.5, to define the interaction between the LO and the RF signals to generate the adequate IF signal that matches the further developed IF adapter circuit. The simulation of the IF adapter ports is indicated in Fig. 6.13, where the integration lines defined in each port have been represented.

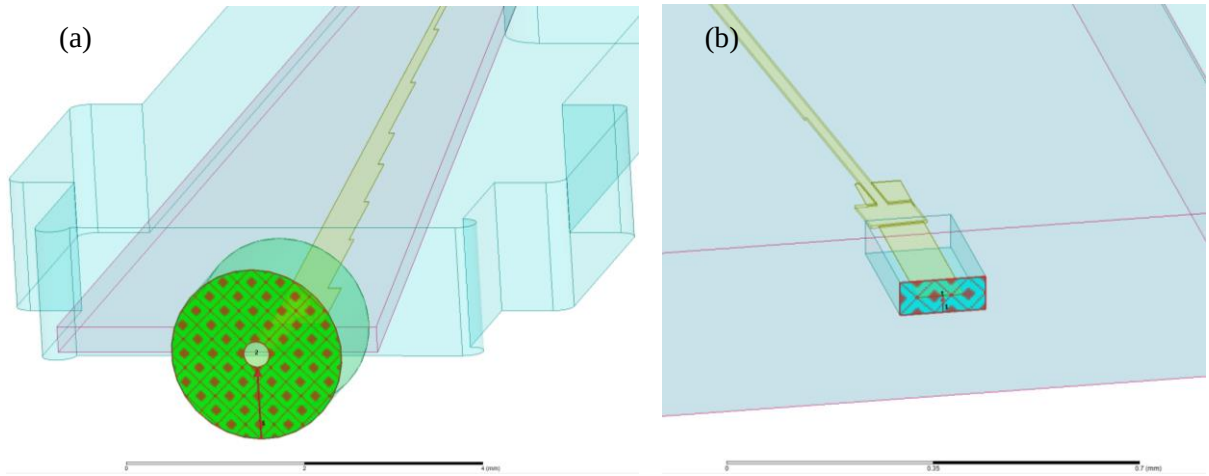

Fig. 6.13. The HFSS design of the 4-8 GHz IF adapter circuit used in the front-end 1200 GHz subharmonic frequency mixer. The 50 Ω (a) port two and the 250 Ω (b) port one simulations have been indicated, where the defined integration lines are represented.

Different ratios between the input and output impedances of the IF adapter circuit can be performed if the MMIC chip has been optimized in accordance with the considered external IF impedance. However, the higher the ratio to adapt, the higher the transmission losses of the signal.

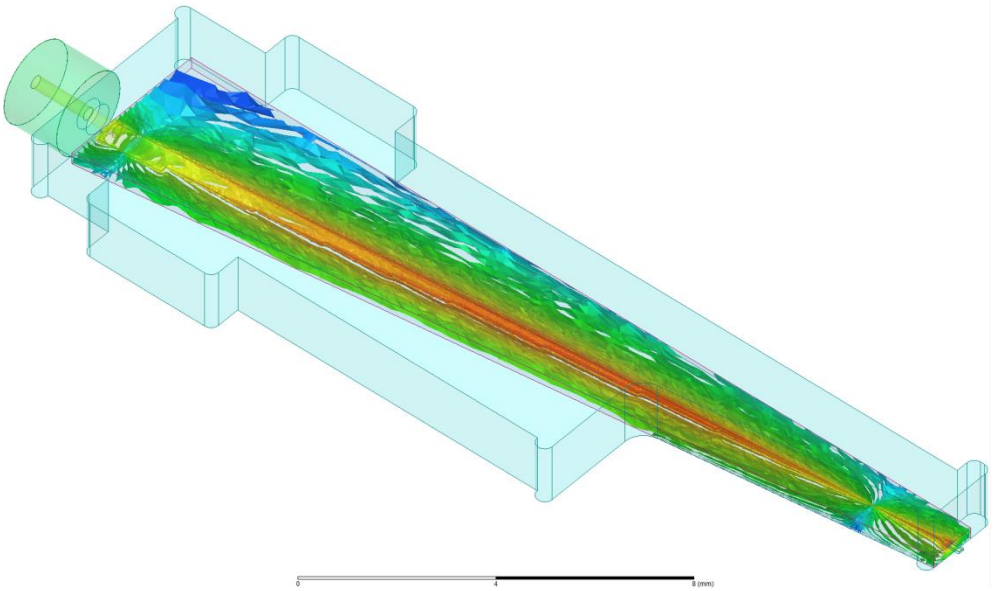

Fig. 6.14. The HFSS simulations of the electric field generated by a 5 GHz IF signal in the IF adapter circuit designed for the 1.2 THz mixer block. The points where the electric field lines converge define half period of the IF signal, and they propagate from the port one to port two.

The influence of the material and thickness of the substrate, where the transmission line is deposited, is very important in the performances of the IF circuit since the electrical permittivity of the substrate defines the confinement of the electromagnetic field inside it. The volumetric electric field distribution in the HFSS simulation of the IF signal at 5 GHz in the quartz substrate of the adapter circuit has been plotted in Fig. 6.14. It is important to note the distribution of the electric field inside the quartz and how its geometry modifies the field lines during one period of the IF signal. The points where all the field lines converge represent half period (~3 cm) of the IF signal that propagates from port one to port two. The higher the permittivity of the substrate, the shorter the required IF adapter length because it is easier to define a high impedance. However, this also introduces higher losses [Poza98, (page 163)]. The thickness of the transmission line is directly related to the skin depth [Poza98, (page 19)] that defines the thickness in which the electric field has decreased in an *e* factor. This allows defining the minimum thickness of the transmission line at certain frequency without compromising its conducting performances. It is possible to calculate the skin depth $\delta = \sqrt{2/\omega\sigma\mu}$ of our gold transmission line at IF frequencies considering a conductivity $\sigma = 45.2 \cdot 10^6$ S/m and permeability $\mu = 4\pi \cdot 10^{-7}$ H/m. It is easy to conclude that 1.7-µm-skin depth is obtained at 2 GHz and 1 µm at 6 GHz. This means that a minimum transmission line thickness ~3.0 µm ensures a decrease of the electric field in a $\sim e^2$ factor for this application to be close to the maximum conduction performances accomplished by the transmission line between 4-8 GHz. A higher transmission line thickness has been defined in the IF adapter circuit presented in Fig. 6.12 in order to ensure the maximum conduction performances in the full IF frequency band, since a lower high frequency conductivity of the gold line is expected. The S-parameters obtained in the HFSS simulation when connecting a 250 Ω load in port 1 (IF input signal) and a 50 Ω load in port 2 (connector) are plotted in Fig. 6.12. The transmission losses S(1,2) in the IF adapter circuit are between 0.2 dB at 3.5 GHz to 0.6 dB at 8 GHz while the return losses S(1,1) are lower than 11 dB in the full IF band and lower than 30 dB in some regions of the band.

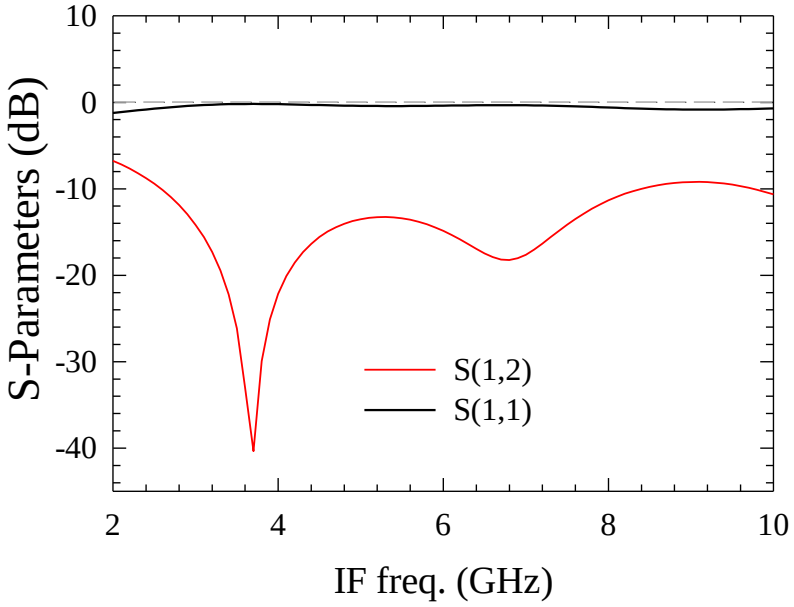

Fig. 6.15. HFSS results of the S-parameters given by the defined IF adapter circuit in Fig. 6.12. A 250 Ω impedance has been defined in port 1 (IF input signal) and 50 Ω in port 2 (connector). The IF transmission in the adapter circuit is between -0.2 to -0.6 dB.

The final dimensions and properties of the proposed IF circuit are mostly based on the knowledge of the materials, the fabrication technology and the operation frequency range rather than in a specific analysis dedicated to the application. In fact, the IF adapter circuit for the 1.2 THz mixer is very similar to the 600 GHz adapter circuit presented in section 5.1.1, since it functions in the same frequency range, adapts the same impedance ratio and uses the same materials.

6.3.2 DC Circuit

The DC circuit in the 1.2 THz mixer design is as simple as possible since it was defined together with the on-chip capacitor defined in the diode cell, presented in Fig. 6.8, to define a series configuration of the diodes for the DC path. This allows biasing with only one voltage power supply and additionally, the separated distribution of the IF and DC simplifies both circuit designs, avoiding complex Bias-T circuits typically used when defining the DC path in the same circuit used to extract the IF signal [Das00]. However, the on-chip capacitor shown in Fig. 6.8 is too small to correctly ground the generated IF signal and it also defines a direct electrical path towards the DC connector. It is therefore necessary to define a complementary ground structure dedicated to the IF signal. This has been accomplished by a grounded capacitance which is connected to the mechanical block in parallel with the DC path. This capacitance behaves as a ground point for the IF signal and as a filter for any voltage noise coming from the power supply source. The value of this plate parallel capacitance is estimated to be at least 1 pF in accordance with the IF frequency and the estimated impedance of the DC cavity in the mechanical block. A 10 pF plate parallel capacitance has been considered in the design to ensure a correct grounding of the IF signal in the DC circuit. This additional plate parallel capacitor is too big to be placed in the proximities of the microelectronic circuit, thus the DC cavity is expanded to make room for this additional lumped elements, as indicated in Fig. 6.11. Regarding the RF and LO signal, most of the signal is expected to be reflected in the ground structure of the MMIC chip, since it was specifically designed for that purpose. Additionally, the increment of the DC cavity dimensions induces high loses for such high frequency signals, which means that any amount of RF or LO signal that reaches the DC circuit is considered to be lost in our simulations.

6.4 Theoretical Comparison in ADS-HFSS Simulations

Comparisons between the estimated performances of the receivers presented in section 6.2 are carried out in this section. Once both designs are finished it is possible to compare their performances under the same conditions defined in ADS-HFSS simulations. Two different analysis are considered in this section, one dedicated to the losses of the LO and RF signals and the conversion losses of the RF signal into the IF signal, and other one dedicated to the noise temperature analysis. The integrated diodes STD model in ADS simulations will be discussed in comparison with the new developed SDD model for the PSBDs. It is important to note at this point the complexity of an integrated noise model in the developed SDD model. This was pointed out by Dr. B. Thomas in [Thom03] and [Thom10b]. The noise in the PSBDs exhibits cyclostationary properties due its dependence on the currents generated by the LO. To determine the exact contribution of this noise source to the equivalent noise temperature of the mixer, the correlation between the large currents generated by the LO must be accounted for. Unfortunately, this correlation is calculated during the harmonic balanced simulation and is not an available result. However, some useful assumptions can be made to estimate the modifications required in the noise temperature generated in the SDD model using the results obtained in the STD model.

The main theoretical considerations used in this section concerning the analysis of mixers performances are discussed before presenting the estimated performances. First, the general concepts of conversion loss of the mixer/receiver is discussed and related with the associated noise temperature of the mixer/receiver. Second, a theoretical technique developed to determine the noise temperature delivered in the IF port by the RF port is discussed. This technique accounts for the relationship between the embedded impedances of the global circuit and the intrinsic impedance of the Schottky diode at each frequency including any possible source of electronic noise in the diode. Third, the way in which these concepts are used in ADS simulations is analyzed and discussed. Finally, the comparison between each 1.2 THz mixer chip presented in section 6.2 is carried out.

6.4.1 Conversion Loss and Noise Temperature of the Receiver

We recall that the term “mixer” refers to any parameter or magnitude coming from the ensemble of the frequency mixer presented in section 4.3. Further, any reference to “receiver” performances points out the introduction of external stages for the IF signal treatment such as the amplification stage or optical systems externally used to lead the RF signal to the mixer antenna. The ensemble of losses in the frequency mixer is the so-called conversion loss of the mixer or the receiver, depending on the considered terms. The conversion loss of the receiver is described by [Pred84] and [Pard16],

$$L_{Rec,SSB} = L_e L_{RF} L_{D,SSB} L_{IF} \,, \tag{6.1}$$

where L_e defines the losses associated to external stages of the receiver (quasi-optical bench, window of a chamber, atmosphere losses, etc), L_{RF} defines the losses suffered by the RF signal when it arrives to the RF antenna of the mixer until it is coupled in the mixer PSBDs, $L_{D,SSB}$ defines the Single Side Band (SSB) conversion losses introduced by the diode cell to transform the coupled RF signal into IF signal. Finally, L_{IF} defines the losses suffered by the IF signal in the chip and the adapter circuit. The ensemble of losses defines the SSB receiver

conversion loss and it is usually expressed in dB. The SSB conversion loss of the mixer can be obtained if the L_e factor is extracted from experimental measurements. The receiver SSB conversion loss can be translated in the SSB noise temperature of the receiver using the expression,

$$T_{Rec,SSB} = (L_e - 1)T_{phy} + L_e T_{Mix;SSB} + L_e L_{Mix,SSB} T_{IF} \,, \tag{6.2}$$

where,

$$L_{Mix,SSB} = L_{Rec,SSB}/L_e \,. \tag{6.3}$$

The term T_{phy} is the physical temperature of the external system (it is the room temperature when measuring at room temperature but is modified in cryogenic measurements), T_{IF} is the noise temperature added by the IF amplifier chain connected to the output IF connector of the mixer. T_{IF} can be easily calculated by eq. 6.6. Finally, $T_{Mix;SSB}$ is the SSB noise temperature of the mixer, which can by calculated using

$$T_{Mix,SSB} = (L_{RF} - 1)T_{phy} + L_{RF} T_{D;SSB} + L_{RF} L_{D,SSB} (L_{IF} - 1)T_{phy} \,, \tag{6.4}$$

where $T_{D;SSB}$ is the SSB noise temperature of the diode cell. It is extremely important to highlight the correct way to define the L_i factors in eq. 6.1 - 6.4. If we know the losses $L_{i;dB}$ expressed in dB (always negative), associated to the *i*-th factor of eq. 6.1, then the way to use these equations is defining [Otos02],

$$L_i = 10^{|L_{i;dB}|/10} \,. \tag{6.5}$$

It has been determined during this work that ADS automatically calculates the SSB and the Double Side Band (DSB) figure noise N_{SSB} and N_{DSB} of the test-bench. It is very useful to correctly account for the transformation of the SSB/DSB noise temperature into the SSB/DSB noise figure using the expression,

$$NF_i = 10 \cdot Log\left(1 + \frac{T_i}{T_0}\right), \tag{6.6}$$

where the noise figure is given in dB, the subscript *i* can be the mixer or receiver accounting for the SSB or DSB noise temperature T_i. It is important to recall that the noise figure is given with T_0= 290 K as a convention and it does not depend on the temperature of the device [Hayk08]. The noise temperature T_i associated usually decreases when reducing the physical temperature of the device, thus it impacts in the noise figure value since the noise temperature of the device is normalized by T_0. This also allows us to calculate the IF noise temperature T_{IF} defined in eq. 6.2 since the experimental LNA used to measure the 1.2 THz mixer has a $NF_{LNA}\approx$ 0.7 dB, which results in $T_{IF}\approx$ 52 K. The magnitudes calculated during ADS simulations are associated to the SSB of the PSBDs spectrum since a single frequency $f_{RF}=f_{LO}+f_{IF}$ is defined in the test-bench to be mixed with the LO signal. However, an equivalent but not identical SSB spectra is obtained in the PSBDs when simulating a $f_{RF}=f_{LO}-f_{IF}$. The precise way to correctly translate the SSB noise of each band side into the DSB noise is given by [Held78],

$$T_{Mix;DSB} = \begin{cases} T_{Mix;SSB}/2 & if \;\; L^{+}_{Mix;SSB} = L^{-}_{Mix;SSB} \\ T_{Mix;SSB}/\left(1 + L^{+}_{Mix;SSB}/L^{-}_{Mix;SSB}\right) & if \;\; L^{+}_{Mix;SSB} \neq L^{-}_{Mix;SSB} \end{cases}, \tag{6.7}$$

where $L^{+}_{Mix;SSB}$ is the SSB mixer conversion loss obtained when simulating $f_{RF}=f_{LO}+f_{IF}$ and $L^{-}_{Mix;SSB}$ is the SSB mixer conversion loss obtained when simulating $f_{RF}=f_{LO}-f_{IF}$. The case

$L^{+}_{Mix;SSB} = L^{-}_{Mix;SSB}$ is typical in our mixing application in the middle of the frequency band but the second definition is required in the edges of the band where $L^{+}_{Mix;SSB} \neq L^{-}_{Mix;SSB}$. It is possible to obtain the correct DSB noise temperature of the mixer in ADS simulations since it has integrated the calculation of the DSB noise figure NF_{DSB}. Regarding the DSB conversion loss, it can be calculated by,

$$L_{Mix;DSB} = \begin{cases} L_{Mix;SSB}/2 & if\ \ L^{+}_{Mix;SSB} = L^{-}_{Mix;SSB} \\ \left(\dfrac{1}{L^{+}_{Mix;SSB}} + \dfrac{1}{L^{-}_{Mix;SSB}}\right)^{-1} & if\ \ L^{+}_{Mix;SSB} \neq L^{-}_{Mix;SSB} \end{cases}, \tag{6.8}$$

where all L_i values are expressed as indicated in eq. 6.5. If eq. 6.8 is transformed into dB, the DSB conversion loss is 3 dB smaller than the SSB conversion loss when $L^{+}_{Mix;SSB} = L^{-}_{Mix;SSB}$.

6.4.2 Noise in Schottky Mixers

We will comment here on a theoretical technique developed to calculate the noise temperature of frequency mixers accounting for the different electronic noise sources in the Schottky diodes and the embedding impendences of the considered mixer circuit. The main noise sources in Schottky diodes are the shot and the thermal noise. An additional noise source associated with the thermal noise generated by hot-electrons in the resistive part of the diodes when pumping with high LO power levels is also mentioned in this section. A brief discussion about each one is carried out. First, it is important to note that the difference between the noise in Schottky diodes and the noise that the Schottky diodes will transfer to the IF load in mixing applications. Theoretical analysis of Schottky diodes noise has been carried out in DC conditions [Gonz97], [Crow87] and in cyclostationary conditions [Shik04], obtaining in any case an equal or lower noise than the pure shot mean-square current noise $\langle i^2 \rangle = 2qI_D$. The Schottky diode noise in cyclostationary conditions has even been experimentally characterized in [Graf10], where the reduction of the noise when pumping with frequency signals is demonstrated. However, it is not the noise that appears in frequency mixing applications, since it is necessary to determine the transferred noise from the RF port of the mixer into the IF port of the mixer when a LO signal puts the Schottky diodes in cyclostationary conditions. The theoretical development of this technique can be found in [Kim61] and [Drag68]. The experimental application of this technique in the analysis of the noise in real frequency mixers can be found in [Held78a], [Held78b] and [Crow87]. The main idea of this technique considers that it is possible to generate the conversion matrix $\boldsymbol{Y'}$ of the diodes [Held78a] admittance from the Fourier coefficients of its capacitance and conductance. This matrix interrelates the sideband frequency components of the small-signal currents and voltages $\delta I'_m$ and δV_m which correspond to frequency components $\omega_m = \omega_{IF} + m\omega_{LO}$ with m= 0, ±1, ±2,…, ±∞, where ω_{IF} is the considered IF frequency of the signal extracted from the IF port and ω_{LO} is the frequency of the local oscillator. It is considered that only the frequency components ω_m can contribute to the noise delivered into the IF port. The equivalent current and voltage sources $\boldsymbol{\delta I' = Y' \delta V}$ where $\boldsymbol{\delta I'_m} = [\cdots, \delta I'_1, \delta I'_0, \delta I'_{-1}, \cdots]$ and $\boldsymbol{\delta V_m} = [\cdots, \delta V_1, \delta V_0, \delta V_{-1}, \cdots]$ are related by the conversion matrix $\boldsymbol{Y'}$. If the matrix relation is transposed $\boldsymbol{\delta V = Z' \delta I'}$, then $\boldsymbol{Z' = (Y')^{-1}}$. The final equation required to determine the noise voltage in the IF output port introduced from the RF input port can be calculated by,

$$\langle \delta V_{i_0}^2 \rangle = \boldsymbol{Z'_0} \langle \boldsymbol{\delta I'_i} \boldsymbol{\delta I'_i}^{\dagger} \rangle \boldsymbol{Z'_0}^{\dagger} , \tag{6.9}$$

where $\boldsymbol{Z'_0}$ is the row of the $\boldsymbol{Z'}$ matrix that corresponds with the impedances at frequencies ω_m with m= 0, ±1, ±2,…, ±∞, obtained from the Fourier coefficients of the admittance and capacitance of the diode junction. $\langle \boldsymbol{\delta I'_i} \boldsymbol{\delta I'_i}^{\dagger} \rangle$ is the correlation function of the noise source *i* (Shot, thermal or hot-electron) and $\langle \delta V_{i_0}^2 \rangle$ is the voltage noise related to the IF port resulting from the statistical average of $\left|\delta V_{i_0}\right|^2$. The different correlation functions that allow calculating the contribution of each noise source in the full mixer noise in accordance with the embedding impedances of the circuit are briefly discussed now.

A. Thermal noise

The correlation matrix for the thermal noise in Schottky diodes is described in [Held78a] by eq. 6.10, where the correlation matrix $\langle \boldsymbol{\delta I'_T} \boldsymbol{\delta I'_T}^{\dagger} \rangle$ is a diagonal matrix because the quasi-sinusoidal components (m,n) $\delta I'_{T_m} = [\cdots, \delta I'_{T_{-1}}, \delta I'_{T_0}, \delta I'_{T_{+1}}, \cdots]$ and $\delta I'_{T_n}$ of the correlation matrix are uncorrelated, since they are not time dependent.

$$\langle \boldsymbol{\delta I'_T} \boldsymbol{\delta I'_T}^{\dagger} \rangle = \text{diagonal} \langle \delta I'_{T_m} \delta I'^{\,*}_{T_m} \rangle = \begin{cases} \dfrac{4k_B T R_{S_m} \Delta f}{\left|Z_{e_m} + R_{s_m}\right|^2} & if \quad m \neq 0 \\ \dfrac{4k_B T R_{S_0} \Delta f}{\left|Z_{e_0} + R_{s_0}\right|^2} & if \quad m = 0 \end{cases} . \tag{6.10}$$

The term *T* in eq. 6.10 is the temperature of the diode, k_B is the Boltzmann constant, *Δf* is the frequency range considered, Z_{e_m} and R_{s_m} are the embedding impedance of the external circuit and the series resistance at frequency ω_m. $R_{s_m} = R_S$ has been considered in our simulations for all *m* values since R_{s_m} refers to any modification of the diodes series resistance associated to frequency dependent phenomena, e.g., the RLC equivalent circuit of semiconductors [Gonz97] together with the saturation phenomena of the electrons [Louh95], [Pard14] and the skin effect [Crow89]. It is important to remark that eq. 6.10 is relating the impedance behavior of the Schottky diode or diodes with the embedding impedances of the circuit at frequencies ω_m to calculate the contribution of the thermal noise generated by the series resistance of the diode into the full mixer noise delivered in the IF port from the RF port when pumping with a specific LO power and bias of the diode.

B. Shot noise

The (m,n) elements of the correlation matrix that describes the correlation between the components of the shot noise at sideband frequencies ω_m and ω_n, where evaluated in [Drag68], as indicated in [Held78a], where I_{m-n} is a Fourier coefficient of the local oscillator exited current signal in the diode.

$$\langle \delta I'_{S_m} \delta I'^{\,*}_{S_n} \rangle = 2qI_{m-n}\Delta f . \tag{6.11}$$

Using eq. 6.11 in eq. 6.9 it is possible to obtain the shot noise contribution to the full mixer noise delivered in the IF port from the RF port when pumping with a specific LO power and bias of the diode.

C. Hot-electron noise

The addition of the hot-electron noise using this formalism can be found in [Crow87]. It proposes an additional DC mean-square current noise source associated to the hot-electron that appears when biasing the Schottky diodes at flat band or above. This term has a square dependence on the current flowing in the diode and the analytical equation that describes the mean-square current noise in DC conditions is given by,

$$\langle \delta I^2 \rangle = \frac{4k_B \Delta f}{Z_S} T_e = \frac{4k_B \Delta f}{Z_S} (T_0 + KI^2) \quad , \tag{6.12}$$

where T_0 is the temperature of the diode. The element K is a constant that depends on the diode properties and geometry as,

$$K = \frac{2\tau_e}{3k_B q \mu N^2 A^2} \quad , \tag{6.13}$$

where τ_e is the average energy relaxation time of the electrons that can be estimated in 1 ps [Zira86], μ is the electron mobility at the doping N and A is the Schottky anode surface. If the Schottky diode is now pumped with a time-dependent signal, eq. 6.12 is transformed into the correlation matrix of the (m,n) components that correlates the thermal and hot-electron noise at sideband frequencies ω_m and ω_n. Since the terms associated to the thermal noise are not time-dependent its influence appears in the diagonal terms of the new (m,n) correlation matrix described in [Crow87] to include the time-dependent hot-electron noise of eq. 6.12 by,

$$\langle \delta I'_{T;hot_m} \delta I'^{\,*}_{T;hot_n} \rangle = \frac{4k_B \Delta f}{\sqrt{Z_{S_m} Z^*_{S_n}}} \Theta_{m-n} \beta_m \beta_n \, , \tag{6.14}$$

where Θ_{m-n} is the (m-n)th Fourier coefficient of the time-dependent term (T_0+KI^2) in eq. 6.12, which is function of the diode current squared. The terms $\beta_i = Z_{S_i} / \left(Z_{S_i} + Z_{e_i} \right)$ for i≠0 and $\beta_0 = Z_{S_0} / \left(Z_{S_0} + Z^*_{e_0} \right)$ comes from the definition of the equivalent noise sources.

The full mixer noise delivered by the RF port, with impedance Z_{e_1}, into the IF port, with an embedding impedance Z_{e_0}, when pumping the Schottky diodes with an specific LO power and DC bias is given by,

$$\langle \delta V^2_{N_0} \rangle = \boldsymbol{Z'_0} \left[\langle \boldsymbol{\delta I'_S \delta I'^{\dagger}_S} \rangle + \langle \boldsymbol{\delta I'_T \delta I'^{\dagger}_T} \rangle \right] \boldsymbol{Z'^{\dagger}_0} \, , \tag{6.15}$$

where it is supposed that there is not a correlation between the shot noise of the junction and the contribution of the resistance with the thermal and the hot-electron noise. The SSB conversion loss of the mixer can be related with the SSB noise temperature using eq. 6.16 in the eq. 6.16, which can be easily concluded from [Held78a],

$$T_{Mix;SSB} = \frac{\langle \delta V^2_{N_0} \rangle}{k_B} \frac{Re\left(Z_{e_0} \right) \cdot L_{Mix;SSB}}{\left| Z_{e_0} + R_{S_0} \right|^2} \, . \tag{6.16}$$

The conversion loss $L_{Mix;SSB}$ in eq. 6.16 contains all the information related to the RF losses in the embedding impedances of the circuit, the conversion into the RF signal in the diode cell and the losses in the IF circuit with the embedding impedance $Z_{e_0} = Z_{IF} = 250\ \Omega$ mentioned in section 6.3.1. $R_{S_0} = R_S$ in our case since a non-frequency dependent series resistance is

normally used. Finally, $\langle \delta V_{N_0}^2 \rangle$ contains all the mean-square voltage noise coming from the losses in the matching network system of the RF and the IF as well as the noise introduced by the Schottky diode cell.

6.4.3 Noise Temperature in ADS Simulations

The procedure described in the previous section is integrated in the ADS simulator but it is not accessible to the users. This means that it is not possible in practice to have access to all the required values of the embedding impedances and values of the (m,n) components of the sideband frequencies in the correlation matrixes of the shot, thermal and hot-electron noises, as already mentioned by Dr. B. Thomas in [Thom03] and [Thom10b]. Additionally, the ADS simulator is not intrinsically coded to deliver this kind of information since it proceeds as indicated in eq. 6.4 to calculate the contribution of the conversion loss L_{RF}, $L_{D;SSB}$ and L_{IF} to the noise temperature of the mixer. In addition, it has the integrated code to calculate the additional contribution of the shot and flicker noise in the term $L_{RF}T_{D;SSB}$.

6.4.3.1 Noise Temperature from the Conversion Loss

The full SSB noise temperature of the mixer is introduced in eq. 6.2 to obtain the SSB noise temperature of the receiver. The SSB noise temperature of the mixer when the value $T_{D;SSB}$= 0 K can be calculated in ADS simulations if the noise contribution of the STD model of the diodes and the series resistances is disabled. In this case let us define the noiseless temperature of the mixer as,

$$T_{0;Mix,SSB} = (L_{RF} - 1)T_{phy} + L_{RF}L_{D,SSB}(L_{IF} - 1)T_{phy}\,, \tag{6.17}$$

which only depends on the RF signal lost in the RF input matching network, the conversion efficiency of the RF signal into IF signal by the diodes and the losses in the IF output matching network. The noiseless temperature of the receiver can be calculated with eq. 6.2,

$$T_{0;Rec,SSB} = (L_e - 1)T_{phy} + L_e\Big((L_{RF} - 1)T_{phy} + L_{RF}L_{D,SSB}(L_{IF} - 1)T_{phy}\Big) + L_eL_{Mix,SSB}T_{IF}\ . \tag{6.18}$$

The value T_{IF} is calculated with eq. 6.6 from the considered noise figure of the LNA. ADS calculates the SSB noise temperature delivered into the IF port, given by the ADS value T_e(IF port number), but it does not calculate the DSB noise temperature. However, the SSB or DSB noise/noiseless temperature of the receiver can be easily calculated in ADS using eq. 6.6 with the automatically calculated values of the receiver noise figures N_{SSB} and N_{DSB}. The SSB noise temperature directly calculated by ADS is the same obtained from the calculated SSB noise figure with eq. 6.6. It is necessary to simulate all the ADS elements of the test bench at the same temperature in order to reproduce the SSB/DSB noiseless temperature of the receiver in ADS. This analysis has been performed and a discrepancy has been noted.

- It was found that an additional ΔT= 360 K constant SSB noise temperature along the simulated frequency band between eq. 6.17 and ADS-2015 results when considering $T_{phy}\approx$ 293 K, and a ΔT= 400 K at $T_{phy}\approx$ 180 K. The origin of this additional SSB noise temperature calculated by ADS-2015 could not be identified since there is not any additional element that can introduce this additional noise temperature value. However, the ADS-2015 noise temperature obtained from the DSB noise figure using eq. 6.6 does

not present the additional ΔT, i.e., the DSB noise temperature obtained from the DSB noise figure calculated in ADS-2015 is lower than half of the SSB noise temperature.

This means that an accurate analysis of the noise temperature of the simulated ADS-HFSS test bench of the receiver starts by comparing the difference between the theoretical SSB noiseless temperature of the mixer given by eq. 6.17 and the directly calculated one by ADS results. This analysis can be useful to estimate how smaller the SSB noiseless temperature of the mixer is supposed to be. However, the DSB noise temperature calculated by eq. 6.6 using the DSB noise figure given by ADS does not present the mentioned ΔT deviation. We can trust the DSB noise temperature value obtained from the DSB noise figure value but the SSB values need to be carefully treated. If we want to carry out a simulation at cryogenic temperatures, it is important to pay attention to the correct value of the LNA noise figure to calculate the term T_{IF} in eq. 6.2. Taking these considerations into account it is possible to ensure that the contribution of the conversion loss of the mixer/receiver in the SSB/DSB noise temperature is correctly determined.

6.4.3.2 Noise Temperature of the Diode Cell

The receiver SSB noise temperature was described in eq. 6.2 in which it is possible to calculate the full noise sources associated to the losses L_e, L_{RF}, $L_{D;SSB}$ and L_{IF}. The losses can be calculated from ADS simulations in both the STD and the SDD model. However, the noise source associated to the Schottky diodes $T_{D;SSB}$ is much more delicate to obtain due to the correlation between the frequency current components of the PSBDs response. The main noise sources in Schottky diodes are the shot noise and the thermal noise. The thermal noise can be simulated in ADS simulations by defining a current noise source in parallel with the series resistance of the diode model (integrated in the lumped resistance model of ADS). The shot noise calculation is supposed to be integrated in the STD model of ADS. An additional noise source, which it is not considered in our analysis, is associated to the hot carriers that can appear in the PSBDs when pumping with high LO input power. It is called the "hot-electron noise" and it is associated to the resistive part of the Schottky diode [Crow87], [Thom10b]. The diodes contribution to the noise temperature given by $T_{D;SSB}$ is deeply discussed in [Pard16] where it is proposed that the SSB noise temperature that a Schottky diode delivers into the IF port of the mixer is given by,

$$T_{D;SSB} = \frac{P_{del} L_{D;SSB}}{k_B \Delta f} \quad , \tag{6.19}$$

where $L_{D;SSB}$ is the diode cell conversion loss and the noise power delivered to the IF port is,

$$P_{del}(f_{IF}) = \frac{S_{IF}(f_{IF}) \cdot Re[Z_e(f_{IF})] \left| Z_{D;SS}(f_{IF}) \right|^2}{\left| Z_{D;SS}(f_{IF}) + Z_e(f_{IF}) \right|^2} \Delta f \quad . \tag{6.20}$$

The value $Z_e(f_{IF})$ is the embedding impedance of the matching network observed by the diodes at the IF frequency signal ($Z_e(f_{IF})$= 250 Ω in our case) while $Z_{D;SS}(f_{IF})$ is the small-signal impedance which relates the fluctuations of the current with the voltage at the terminals of the diodes at IF frequency. It can be determined by exciting the diode with a voltage perturbation at IF frequency superimpose to the large voltage LO signal that has been excited by the LO power. In ADS simulations it corresponds with the quotient of the simulated I(t) and V(t) spectra of each Schottky diode and the full $Z_{D;SS}(f_{IF})$ of the diode cell is obtained

after consider the parallel configuration of both impedances. The value of $|Z_{D;SS}(f_{IF})|$ is around 175 Ω in our designed chips with a very small imaginary part, similarly to results presented in [Pard16]. It is reasonable since the chips were optimized to deliver the IF signal into a real IF port impedance $Z_e(f_{IF})$= 250 Ω. The diode $S_{IF}(f_{IF})$ is the most critical value to be determined.

The properties of the Schottky diode noise temperature $T_{D;SSB}$ described by eq. 6.19 and 6.20 are especially useful for us when comparing the noise temperature of the receiver predicted by the STD and the SDD models. The excited voltage signal in the PSBDs by the LO oscillator power is very similar in both models and we can assume that the spectral noise at IF frequency $S_{IF}(f_{IF})$ is very similar in both diodes. In addition, if a constant $P_{del}(f_{IF})$ value is assumed for a certain LO input power and diodes bias in both the STD and the SDD model, it is possible to conclude that the difference of the Schottky diode noise temperature $\Delta T_{D;SSB}$ calculated between the STD and the SDD model, is linearly related with the difference in the conversion efficiency of the diodes $L_{D;SSB}$. We can correctly compare in this way the predicted SSB/DSB noise temperature of the receiver predicted by the STD and the SDD models by using the simulation results obtained with the integrated noise model in the STD model of ADS.

6.4.4 Simulated Conversion Loss in the 1.2 THz Mixer Chips

The conversion loss performed by each 1.2 THz mixer chip presented in section 6.2 is analyzed in this section. The different elements L_e, L_{RF}, $L_{D;SSB}$ and L_{IF} are compared in different input LO power and bias of the diodes using the integrated STD model in ADS and the developed SDD model. The substrate effect explained in Section 2.2.4.2 appears in these PSBDs due to the reduced thickness of the epilayer. The influence of this phenomena in the conversion loss of the device is therefore analyzed. The comparison between the pure series resistance model and the RLC series impedance model are also discussed in this section.

6.4.4.1 ADS-HFSS Test Bench of the 1.2 THz Receiver

First of all, we will describe the defined ADS-HFSS test bench in order to clearly calculate the conversion losses L_e, L_{RF}, $L_{D;SSB}$ and L_{IF}. The procedure discussed in section 2.3 is used. The input LO and RF signal are defined with a one-tone power source frequency domain ADS element, where the LO and the RF input power is defined. The impedance of each port source is defined by the TE_{10} impedance of the waveguide in accordance with the dimensions of the waveguide and the frequency of the propagation signal, given by [Poza98, Section 3.3],

$$Z_{TE_{10}} = \frac{k\eta}{\beta_{10}} = \eta\left(1-\left(\frac{c}{2af}\right)^2\right)^{-1/2} = 120\pi\frac{2b}{a}\left(1-\left(\frac{c}{2af}\right)^2\right)^{-1/2}\ \Omega\ , \qquad (6.21)$$

where $\eta = \sqrt{\mu/\varepsilon}$ is equal to 120π Ω in free space, a and b are the height and the width of the waveguide respectively, c is the light speed and f is the frequency of the propagation signal. A circulator ADS element is used in the LO and RF ports to measure the reflected LO and RF power signal. A 0.4 dB attenuator ADS element is defined in the RF input matching network to represent the losses in the RF antenna. The HFSS simulated waveguides walls (mechanical block) and the ADS waveguide section model are always simulated by considering a gold conductivity σ= $2\cdot10^7$ S/m lower than the dc value and relative permeability μ_r=0.99996

[Lamb96]. The LO and RF signals are connected to the corresponding simulated HFSS S-parameters box, which represents the simulated structure of the MMIC chip with the input waveguide matching network of the LO and RF signals. A 5 port S-parameter is used in this test bench for both, the LO and the RF. The ports 1 and 2 correspond to the diode 1 and diode 2, the port 3 is associated to the DC port of the chip, the port 4 is associated to the input LO or RF signal and the port 5 is associated to the IF port. The PSBDs diodes are connected to the ports 1 and 2 of each 5-port S-parameters. The generated response of the diode cell is additionally connected to a 4-port S-parameters associated to the third harmonic of the LO signal. The third LO harmonic leaves the diode cell due to the antiparallel configuration of the diodes and the correct embedding impedance is required in order to have the correct harmonic and intermodulation products generation. The higher harmonics are connected to a 50 Ω load. It was concluded during this work that the third LO harmonic is high enough to modify the harmonic and intermodulation products generation if it is connected to the 50 Ω load. The diodes response is also connected to a 4-port S-parameter where the IF adapter circuit presented in section 6.3 is simulated at IF frequencies. The port 1 and 2 are connected to the diodes to extract their IF signal response, the port 3 is connected to the DC circuit and the port 4 is connected to the IF circuit. A 10 mm-length-50 Ω-impedance transmission line model is simulated in ADS to represent the coaxial connectors used to lead the IF signal to the LNA, but the losses associated are very low. A LNA is included in the ADS test bench where it is possible to define the LNA noise figure to simulate the additional noise temperature associated to the amplification stage of the full receiver. A Miteq 4-8 GHz LNA with noise figure NF_{LNA}= 0.7 dB is used to experimentally characterize this device as well as the 600 GHz mixer presented in [Treut16].

The simulated diode properties features a A= 0.2 μm^2 Schottky anode surface with a W_{EP}= 55 nm epilayer thickness doped at N_{EP}= 3·10^{17}cm^{-3} and a built-in voltage V_B= 0.75 V. The definition of the C-V characteristic in the STD model is limited to the definition of the junction capacitance C_{j0}= 0.52 F at the considered built-in voltage. The developed SDD model of the diode defines the C-V characteristic, as explained in Section 2.2.4, from the geometry of the anode L_{SCH} and L_1, and it uses the epilayer thickness to automatically define the series resistance value. The substrate effect parameters W_{CA}= 28 nm and W_{CB} = 9 nm are used in this analysis to relate then with the epilayer thickness and finally define the impact of the substrate in the C-V characteristic of the PSBDs. The considered nominal series resistance is R_S = 86 Ω for the pure series resistance model indicated in Fig. 2.4. The RLC series impedance model uses the R_S series resistance distributed between a R_{int} and R_{ext} resistances, where R_{int} is the series integrated in the RLC circuit to represent the internal series impedance of the epilayer and R_{ext} is used in series configuration to represent any other resistance source of the Schottky junction. The L_{int} and C_{int} values are calculated as described in section XX using the internal resistance R_{int}. Around half of the experimental series resistance in DC conditions has been observed in 2D-MC simulations of equivalent PSBD structures. It is the reason why the relationship $R_{int} \approx R_{Ext}$ is used with $R_S = R_{int} + R_{ext}$.

6.4.4.2 SSB Conversion Loss of the 1.2 THz Receiver

The conversion loss obtained in ADS-HFSS simulations of the 1.2 THz mixer chips presented in section 6.2 is carried out in this subsection in order to determine the most adequate mixer chip design for this application. All elements in the ADS simulator are simulated in the same way for both designs but the simulated S-parameters corresponds with the HFSS simulations of the corresponding MMIC chip. The DC circuit has been simulated in the LO, 3LO and the RF S-parameters ADS element and it is connected to a matched load to simulate the loss of any LO, 3LO and RF power that goes through the DC path. We recall again that the ground structure presented in section 6.2 was specifically optimized to ground the LO and the RF, and due to the dimensions of the DC cavity the LO and the RF signals cannot propagate inside it. The diodes have been defined under the same conditions and with the same properties. No RLC circuit is considered in this first analysis since it does not modify the conclusions of this comparison. It is necessary to analyze the different terms of eq. 6.2 to determine the performance of each chip. The SSB conversion loss of each chip, simulated with the STD (dashed lines) and the SDD (solid lines) model, has been plotted in

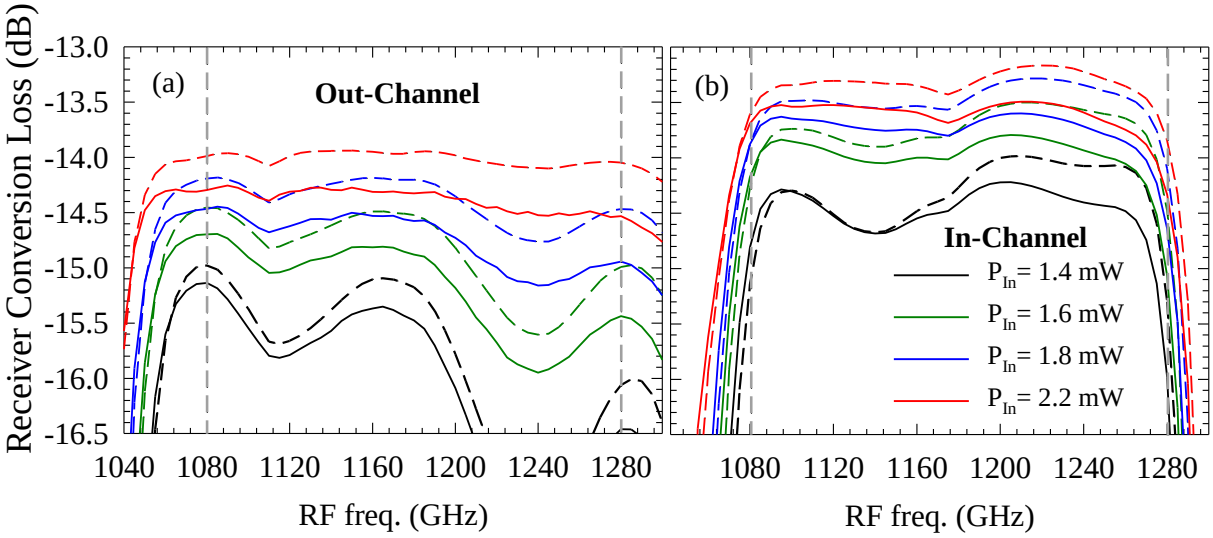

Fig. 6.16. ADS-HFSS results of the SSB conversion efficiency at 5 GHz of IF signal of both (a) the out-channel and (b) the in-channel design. The ADS-HFSS test bench of each receiver has been tested with a LO power sweep from 1.4 mW to 2.2 mW without biasing the diodes. The STD model (dashed lines) and the SDD model (solid lines) have been compared here.

It is possible to appreciate some important aspects of the general behavior of each developed mixer design. The out-channel chip presents a very large frequency band compared to the in-channel chip. It was very hard to get the required frequency band in the in-channel design and there is a high risk to lose the upper and the bottom frequencies of the band. Regarding the net values of the SSB conversion loss performed by each design, the in-channel design performs a conversion efficiency up to 0.8 dB better than the out-channel chip in some point of the frequency band. However, it does not necessarily mean a better noise performance since it is possible to appreciate in eq. 6.4 that the noise contribution is distributed differently between the elements L_{RF}, $L_{d,SSB}$ and L_{IF}. The $L_{IF} \approx 0.45$ dB term is almost constant in the full band for all the values of the LO power sweep in both designs, since it is the same IF adapter circuit

and the chips where optimized for delivering the IF signal to the same embedding IF impedance.

Now we compare the contribution of elements L_{RF} and $L_{d,SSB}$ to the global $L_{Mix;SSB}$. The factor L_{RF} is plotted in Fig. 6.16, where the RF coupling efficiency has been used in eq. 6.5 to obtain the dimensionless factor. It is possible to appreciate again the higher bandwidth covered by the out-channel design, but it also has higher losses in the RF path. Regarding the difference between the diodes model, it has obtained very similar results between both RF coupling capabilities. The only difference is a higher negative slope predicted by the STD model than in the SDD one, i.e., the SDD model predicts a slightly higher loss of the RF signal at higher frequencies of the band and lower, or similar, at the low frequencies.

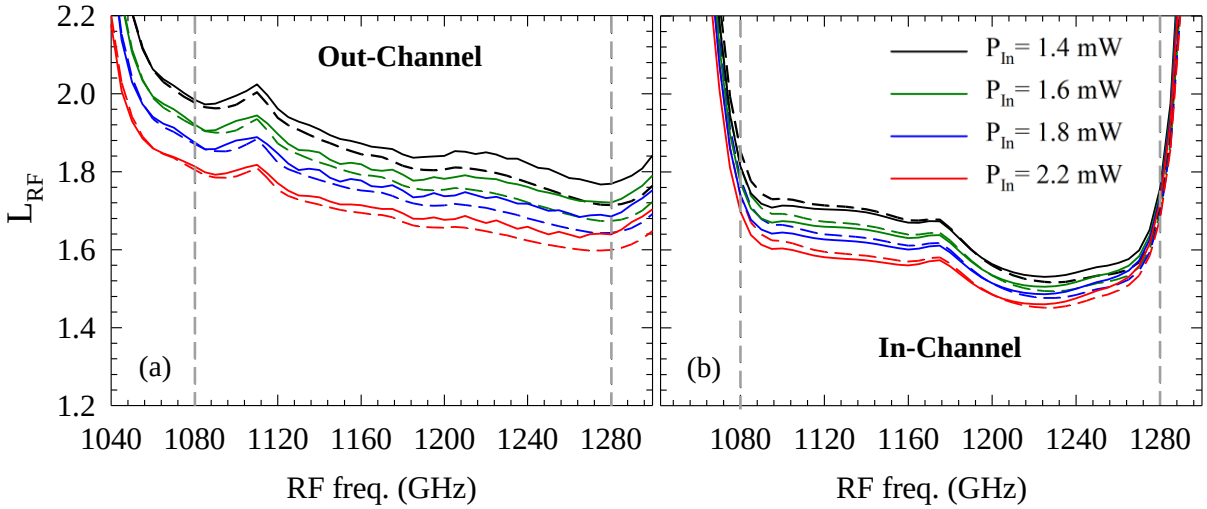

Fig. 6.17. ADS-HFSS results of the RF coupling efficiency at 5 GHz of IF signal expressed in terms of the dimensionless factor L_{RF} for both (a) the out-channel and (b) the in-channel design. The ADS-HFSS test bench of each receiver has been tested with a LO power sweep from 1.4 mW to 2.2 mW without biasing the diodes. The STD model (dashed lines) and the SDD model (solid lines) have been compared here.

The equivalent analysis is carried out in Fig. 6.18 to obtain the $L_{d,SSB}$ from the conversion efficiency of the diode cell to generate the IF signal using the coupled RF signal.

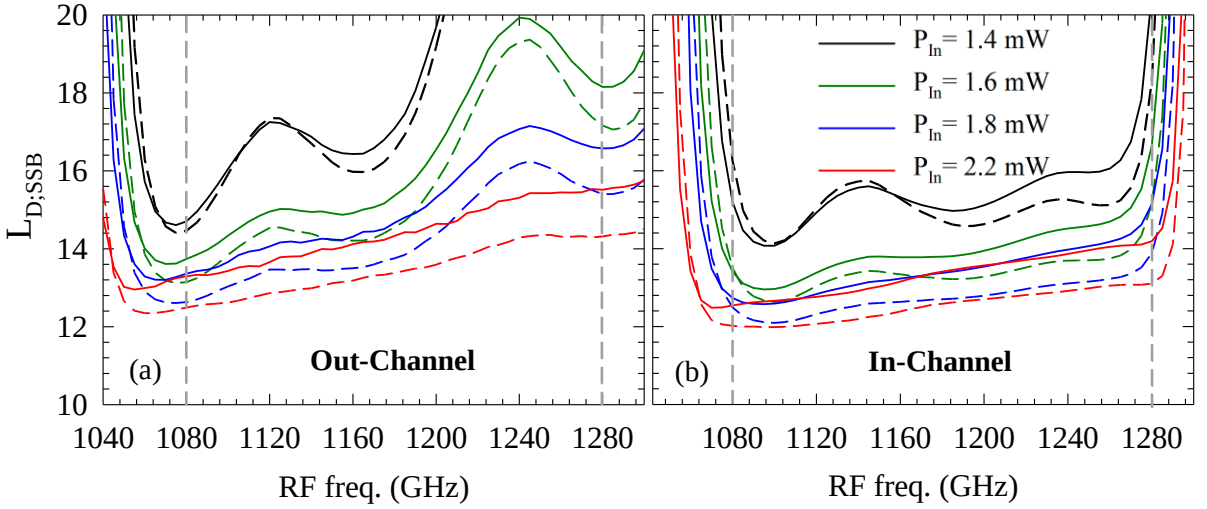

Fig. 6.18. ADS-HFSS results of the SSB conversion efficiency of the diode cell at 5 GHz of IF signal expressed in terms of the dimensionless factor $L_{D;SSB}$ for both (a) the out-channel and (b) the in-channel design. The ADS-HFSS test bench of each receiver has been tested with a LO power sweep from 1.4 mW to 2.2 mW without biasing the diodes. The STD model (dashed lines) and the SDD model (solid lines) have been compared here.

The SSB conversion efficiency of the diode cell in the in-channel indicated in Fig. 6.18 performs more efficiently than the out-channel design to generate the IF signal from the coupled RF signal indicated in Fig. 6.17. It is additionally able to perform a more stable conversion efficiency when reducing the available LO power, since the conversion efficiency in the out-channel chip is completely lost in half of the frequency band when the LO power is reduced down to 1.4 mW and no bias is applied in the diodes. Additionally, the bandwidth of the conversion efficiency in the in-channel design is large enough to correctly cover the required frequency band, but it useless since the RF signal is not correctly coupled at the edges of the band. The better conversion efficiency of the in-channel chip can be explained due to the shorter bandwidth required during the optimization process. This is because the difficulty observed in the RF coupling of the in-channel chip allowed the diode cell to be better matched with the reduced bandwidth of the coupled RF signal and it therefore induces a better conversion efficiency of the diode cell. In the opposite case, the easy RF coupling observed in the out-channel design allowed the diode cell to increase as much as possible the frequency band where a good conversion efficiency is performed, at expenses of a reduction of the conversion efficiency. Regarding the predicted results by each model, the SDD model predicts a lower conversion efficiency (higher $L_{d,SSB}$) than the STD model in spite of having exactly the same I-V characteristic. It is probably associated to the higher capacitance observed by the excited LO voltage signal during the part of the period where the depletion region of the diode is depleting the substrate layer, which is accounted for in the SDD model.

We complete the discussion related to the conversion loss of each 1.2 THz mixer presenting the L_{LO} factor in Fig. 6.19, which represents the LO coupling efficiency of the device. This factor has been calculated from the ratio between the input LO power in the mixer block and the amount of LO power coupled in the diode cell. The dimensionless factor has been calculated with eq. 6.5.

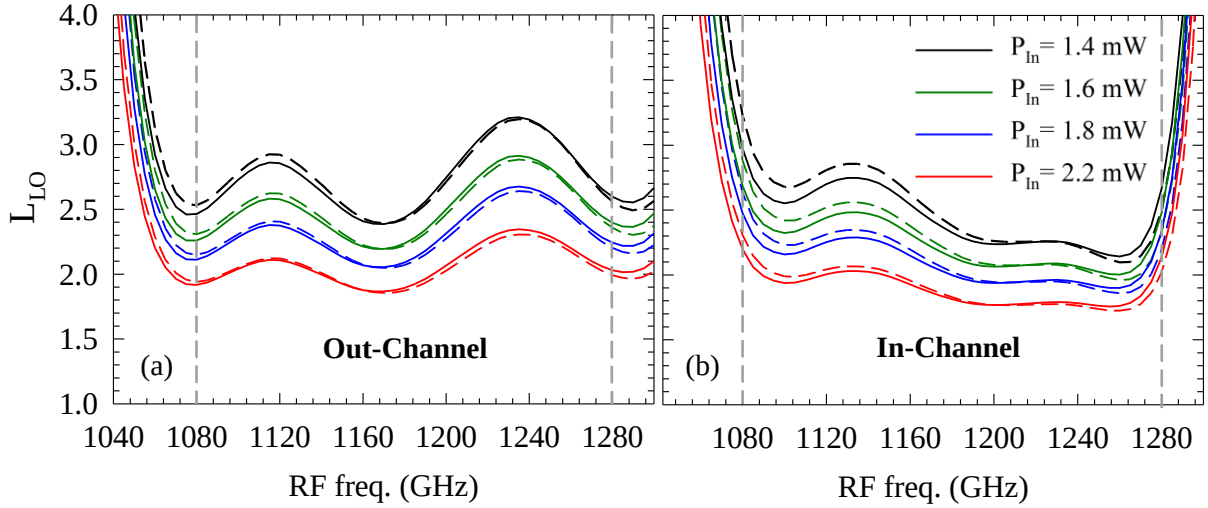

Fig. 6.19. ADS-HFSS results of the LO coupling efficiency at 5 GHz of IF signal expressed in terms of the dimensionless factor $L_{D;SSB}$ for both (a) the out-channel and (b) the in-channel design. The ADS-HFSS test bench of each receiver has been tested with a LO power sweep from 1.4 mW to 2.2 mW without biasing the diodes. The STD model (dashed lines) and the SDD model (solid lines) have been compared here.

The LO coupling efficiency is quite similar in both designs but the in-channel design performs again at a reduced bandwidth compared to the out-channel design. Regarding the predictions of each model, the coupled LO power is very similar for both models in the out-

channel design while there are some differences at the low frequencies of the in-channel design, where the SDD model predicts a slightly better coupling efficiency than the STD one.

We can finally conclude that the origin of the higher value of the SSB conversion loss predicted for the in-channel receiver design in Fig. 6.16, comes from the smaller RF conversion efficiency L_{RF} factor and especially from the diode cell SSB conversion efficiency $L_{D;SSB}$ factor. The adjusted bandwidth of the RF frequency coupling performed by the in-channel design puts in risk the specifications required by the SWI instrument at the edges of the frequency band of the receiver. The spectral line of the methane at this frequency range, in which this channel is interested in, is placed around ~41 cm^{-1} wavenumber ($f_{RF} \approx$ 1240 GHz) as indicated in [Wish02]. Other interesting compounds with spectral lines in the frequency range of this receiver are analyzed in [Webs05].

6.4.5 Simulated Noise Temperature in the 1.2 THz Mixer Chips

The required conversion loss factors L_{RF}, $L_{D;SSB}$ and L_{IF} have been discussed and calculated in the previous section. These values allow us to analytically calculate the SSB and DSB noiseless temperature of the receiver by using eq. 6.18. The noiseless temperatures of each receiver are discussed and compared in this section. The contribution of the diode cell to the final SSB and DSB noise temperature of the receiver, given by eq. 6.2, is then obtained by comparing the ADS-HFSS results obtained with the STD integrated noise model of the diodes and the analytical noiseless temperature given by eq. 6.18. The assumption of an equivalent contribution of the diodes to the SSB noise temperature $T_{D;SSB}$ in both models is evaluated in this section. This assumption is based on two points. First, a very similar LO coupling efficiency has been shown in Fig. 6.19 when pumping with the same LO input power. Second, the current noise spectra of the Schottky diode cell is defined by the excited LO voltages signal, as demonstrated in [Pard16]. Similar noise contribution can therefore be expected from the STD model and the SDD model since a very similar LO power is coupled when considering each different model. However, a very important discussion about the validity of this study is required before presenting the noise temperature predictions.

The noise model of the STD Schottky diode model in ADS is enabled and a thermal noise associated with a series resistance around half of the simulated series resistance R_S for each diode is considered in our diode cell noise contribution. This analysis of a lower series resistance value considered for the thermal contribution of the diode cell is used in accordance with the satisfactory comparisons carried out during this work with the 600 GHz mixer presented in chapter 4 (this analysis is not included in this work). This is a phenomenological consideration that does not have a precise base but can be easily understood based on two main considerations. On one hand, a noise contribution of the Schottky diodes has been demonstrated to be equal or lower than the pure shot 2qI noise, found in [Gonz97], [Shik04], [Graf10] and [Pard16]. This means that the simulation of the full thermal noise associated to the simulated series resistance in ADS could be considered as a maximum reference. On the other hand, an extremely simple model of the flat band conditions is considered in our LEC model, which is essentially led by the alpha term in the definition of the C-V in the proximities of flat band. Neither model can account for saturation phenomena nor the hot-electron noise associated to hot-electrons. These two additional phenomena are completely

required in mixers, especially at this frequency range, and they are expected to deviate the I-V characteristic measured in DC conditions from the *I(t)* characteristic that the real diodes will have in cyclostationary conditions at the LO frequency [Schl01b]. This author has even considered the absence of self-heating of the Schottky diodes during the LO cycles. The final real SSB conversion loss of the diodes $L_{D;SSB}$ and the real voltage and current response excited by the LO signal in the diode cell, should therefore deviate from the results presented in this virtual analysis. This means that a precise analysis of the diode cell noise contribution is useless since the required base to carry out such a precise comparison is not available. The introduction of more or less thermal noise from the series resistance can be used to fit the experimental results in order to accounting for the unconsidered phenomena, but it is important to make clear that the $L_{D;SSB}$ is also an approximation of the experimental performances. Although there are many challenges to address before having a good Schottky model to carry out a sound base mixers comparison, it is possible to determine the impact of the SDD junction capacitance model in the conversion loss and the noise temperature of the receiver when comparing with the STD model, since they are compared under the same conditions. We can also trust in the compared performances obtained in each designed 1.2 THz mixer since they are compared under the same conditions.

The SSB noise temperature in the diode cell has been obtained by extracting the noiseless temperature $T_{0;Rec;SSB}$ of eq. 6.18 from the noise temperature $T_{Rec;SSB}$ of eq. 6.2, given by ADS with the STD model. Results of the obtained SSB noiseless temperature of the receiver have been plotted in Fig. 6.20 for both designs of the 1.2 THz mixer. The SSB noiseless temperature has been obtained using the eq. 6.18 with the values secured from Fig. 6.16 to Fig. 6.18. A lower SSB noiseless temperature of the receiver has been obtained in the in-channel design in accordance with the lower values of $L_{d,SSB}$ and L_{RF} secured in previous section. The in-channel receiver also performs a more stable noise temperature when reducing the available LO power, but the reduced frequency band compared with the out-channel design still induces a high risk in the feasibility of these performances at the edges of the band.

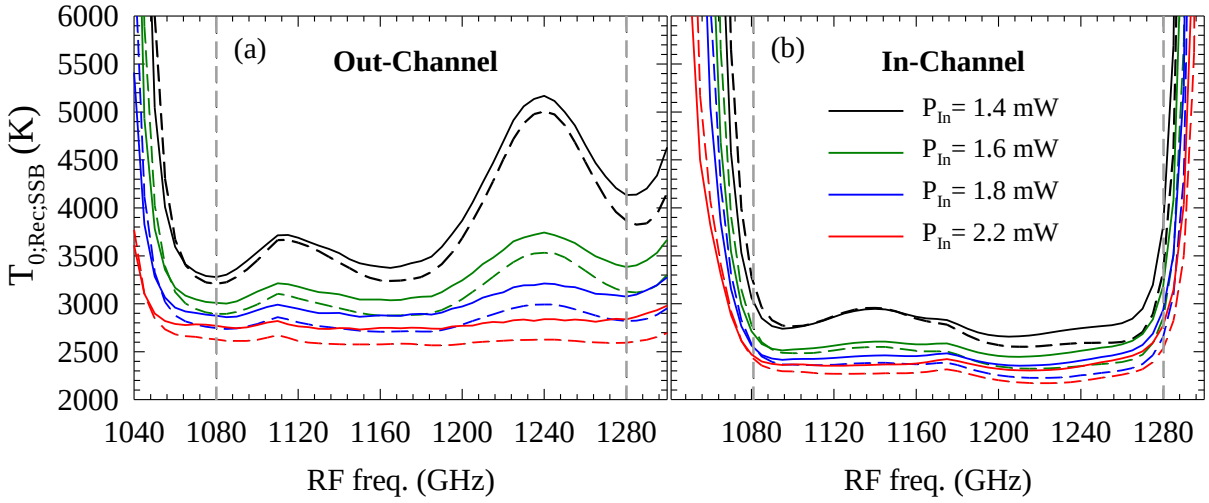

Fig. 6.20. ADS-HFSS results of the analytical SSB noiseless temperature of the receiver $T_{0;Rec;SSB}$ calculated at 5 GHz of IF signal with eq. 6.18 for both (a) the out-channel and (b) the in-channel design. The ADS-HFSS test bench of each receiver has been tested with a LO power sweep from 1.4 mW to 2.2 mW without biasing the diodes. The STD model (dashed lines) and the SDD model (solid lines) have been compared here.

The impact of the considered Schottky model does not dramatically modify the value of the noiseless temperature. It only indicates a global increase of the noiseless temperature that slightly increases at the high frequencies of the band. We can use the results obtained in Fig. 6.20 to identify the SSB noise temperature contribution of the diode cell calculated by the integrated ADS simulations of the shot noise and the thermal noise. We recall again that the full series resistance R_S= 86 Ω has been considered in the electrical response of the PSBDs, but it only considers half of the resistance in the thermal noise contribution. The results of the SSB noise temperature contribution of the diodes $T_{D;SSB}$ calculated by ADS under the discussed definition is plotted in Fig. 6.21. The obtained $T_{D;SSB}$ is assumed to be the same in the STD and the SDD model.

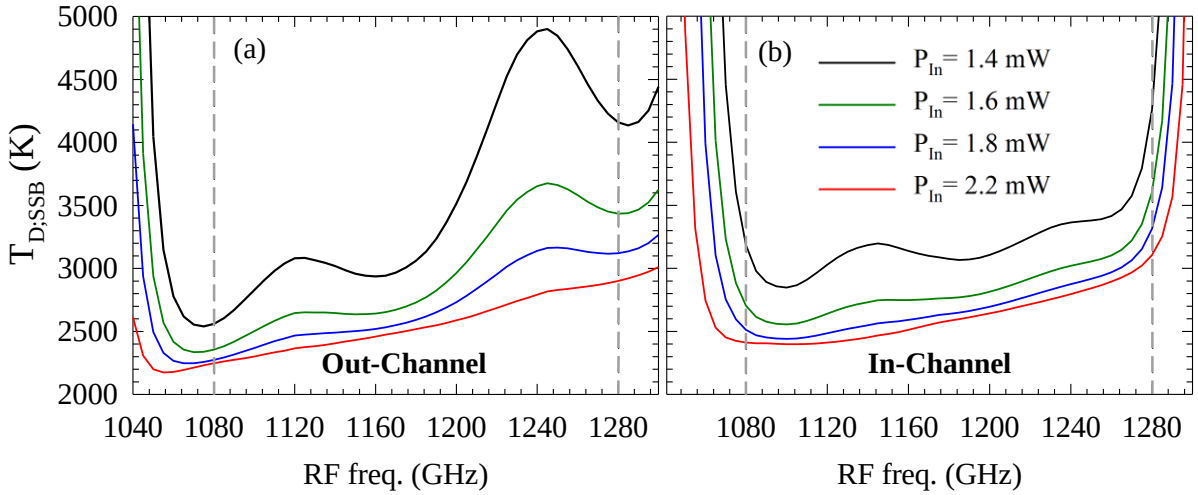

Fig. 6.21. ADS-HFSS results of the SSB noiseless temperature contribution of the diode cell $T_{D;SSB}$ calculated at 5 GHz of IF signal with the difference between eq. 6.2 and 6.18 for both (a) the out-channel and (b) the in-channel design. The ADS-HFSS test bench of each receiver has been tested with a LO power sweep from 1.4 mW to 2.2 mW without biasing the diodes. The same $T_{D;SSB}$ contribution is considered in both the STD and the SDD model.

It is possible to conclude in Fig. 6.21 a very important contribution of the diode cell to the noise temperature of the receiver since the presented value of the $T_{D;SSB}$ is already as high as the noiseless temperature associated to the conversion loss. Additionally, the final contribution to the noise temperature of the receiver is given by the term $L_{RF}{\cdot}T_{D;SSB}$ that makes the diode cell contribution more important than the rest of contributions indicated in eq. 6.18. An indetermination in the predicted SSB noise temperature of the receiver is introduced by the way in which the noise contribution of the diode cell has been defined. Regarding the results obtained in Fig. 6.21, a lower SSB noise temperature contribution of the diode cell in the out-channel design is observed in Fig. 6.21, and the in-channel design is still more stable when reducing the available input LO power since it is directly associated with the conversion loss of the diode cell $L_{D;SSB}$. The contribution of the diode cell to the noise temperature is correctly covering the full frequency band in both designs, but the lower RF and LO coupling observed in Figs. 6.17 and 6.19 degrades the bandwidth of the in-channel design.

The final predicted DSB noise temperature performances of each 1.2 THz receiver design are plotted in Fig. 6.22 for each model. The final DSB noise temperature of the receiver is directly obtained from ADS simulations of the STD model while the predicted value for the

SDD model has been obtained when adding the corresponding additional $L_{RF}{\cdot}T_{D;DSB}$ contribution to eq. 6.18.

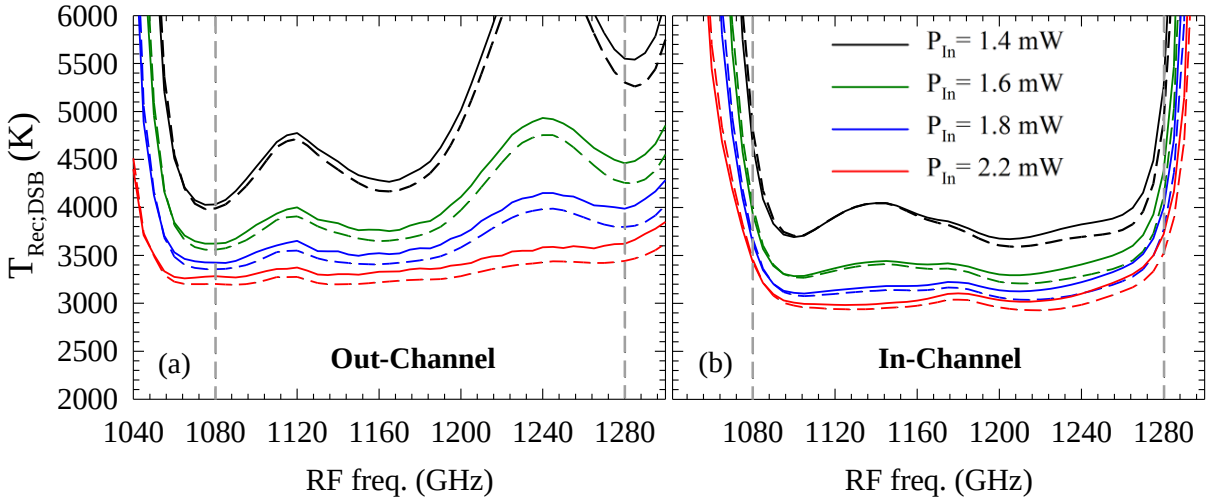

Fig. 6.22. ADS-HFSS results of the DSB noise temperature of the receiver $T_{Rec;DSB}$ at 5 GHz of IF signal for both (a) the out-channel and (b) the in-channel design. The ADS-HFSS test bench of each receiver has been tested with a LO power sweep from 1.4 mW to 2.2 mW without biasing the diodes. The STD model (dashed lines) and the SDD model (solid lines) have been compared here. The simulations consider room temperature conditions.

The results presented in Fig. 6.22 are the most important when optimizing a frequency mixer since it is the real value experimentally measured and it is accounting for the noise temperature of the elements that, together with the mixer noise temperature, contribute to the noise temperature of the receiver. The objective of the optimization is to reduce the DSB noise temperature of the receiver as much as possible. The results obtained in Fig 6.22 together with the discussion concerning the validity of this information indicates that a DSB noise temperature higher than 3250 K and lower than 4000 K can be expected in an experimental receiver based on the out-channel mixer design and around 250 K reduced range for the in-channel design. The DSB noise temperature of the in-channel design of the 1.2 THz receiver is expected to have lower LO input power requirements and a few hundreds of Kelvins lower than in the out-channel design, but it is only true in the middle of the band. The reduced bandwidth of the in-channel design, due to the higher constrains of this design, presented in Fig. 6.4, for the LO and the RF coupling makes the performances at the edge of the band very hard to experimentally obtain since any fabrication defects in the diode cell and the matching network of the mechanical block will directly impact the RF and the LO coupling at the edges of the band. It would be possible to redesign the in-channel structure to cover a wider frequency band at the expense of an increment of the final DSB noise temperature. However, this study has demonstrated that the design considerations and time requirements of the out-channel design are notably reduced. PICK UP HERE THE CORRECTIONS The wide and flat bandwidth performed by the out-channel design is relatively simple to obtain once the diode cell structure is correctly defined to efficiently couple the LO and the RF signals while it correctly defines their ground path. The separated RF filtering from the LO and RF diode cell matching makes the increment or reduction of the desired bandwidth a simple process. Additionally, the reduced utilization of split line sections makes it possible to fabricate a non-bias version without degrading the transmission

characteristics of the LO and the RF paths. Regarding the in-channel design, modifications of the diode cell structure were required and a significant amount of combinations of the transmission lines design, used in the middle channel, were required to reduce the DSB noise temperature as much as possible. The introduction of the split line to define the bias path in the in-channel design also introduces the presence of an additional TEM mode propagated between the two metals of the split line. This split line introduces some additional losses and it defines the way in which the LO and the RF signals are transmitted in the ground section (Fig. 6.7) and these losses cannot be avoided if a non-bias version is fabricated. Additionally, the elimination of the on-chip capacitances in the diode cell and the ground structure could probably modify the impedance matching in one side of the frequency band (more probable the high one).

We conclude this study with the idea that the out-channel design is more suitable for our application since it ensures a wider bandwidth. This means that the required bandwidth of the 1.2 THz for SWI will be much easier to obtain when accounting for the experimental fabrication defects of the MMIC chip and the mechanical block. Since the dimensions of the RF input waveguide b_{RF} (Fig. 6.9) is only 90 μm and the deviation of the mechanical block fabrication process is up to ±10 μm, it is a certainty that the mechanical block will be full of deviations from the nominal design. An analysis of the impact of these deviations has been carried out in the simulated matching network of the mechanical block in HFSS and it always has a direct impact on the bandwidth of the receiver, especially at high frequencies.

6.4.6 Analysis of the Bias Performances and the RLC Equivalent Circuit

The introduction of the RLC circuit discussed in section 2.2 will now be analyzed in the defined ADS-HFSS test bench of the 1.2 THz out-channel version of the mixer. The out-channel version is used from this point in the rest of this section since all the efforts of LERMA were placed on this design to accomplish the demonstration of the prototype. The DSB noise temperature performances of the out-channel 1.2 THz receiver are reviewed now when analyzing the presence of a DC bias in the diode cell. The STD model is used in the simulations described in this section since the SDD model have not proven to dramatically modify the performances and the STD model has the noise model of the diodes integrated. The analysis is focused on the DSB noise temperature performances along the frequency band and the impact of the available LO input power on these. This section starts with the analysis of the bias in the DSB noise temperature performances and finishes with the impact of the RLC circuit.

6.4.6.1 Impact of the Bias

The biasable MMIC chip of the mixer was designed to mitigate the impact of a low LO input power, especially at the edges of the band. The presented designs in section 6.2 were optimize to use 1 mW of LO power as efficiently as possible, since it was expected to be difficult to obtain. The experimental results of the 600 GHz two anodes doubler presented in section 4.1 and the improved version of this doubler presented in section 4.2 have opened the possibility of a non-biasable version of the mixer, since the bias becomes unnecessary when pumping between 1.8 mW to 2 mW of LO input power in ADS-HFSS simulations. A constant

series resistance model is used to analyze the impact of the bias in the global performances since the conclusions will not be modified by the introduction of the RLC equivalent circuit. We recall the simulated parameters in the STD diode model to represent as close as possible the real PSBDs. The simulated I_{Sat}= 0.682 pA, V_B= 0.75 V, C_{j0}= 0.518 fF, α= 0.85, η=1.38 and R_S= 86 Ω.

The DSB noise temperature of the out-channel 1.2 THz mixer when pumping the receiver at 1 mW LO input power and sweeping the bias of the diodes from 0 V to 0.6 mV is plotted in Fig. 6.23(a) and an analysis of the impact of different bias when sweeping the LO input power at a specific frequency is plotted in Fig. 6.23(b).

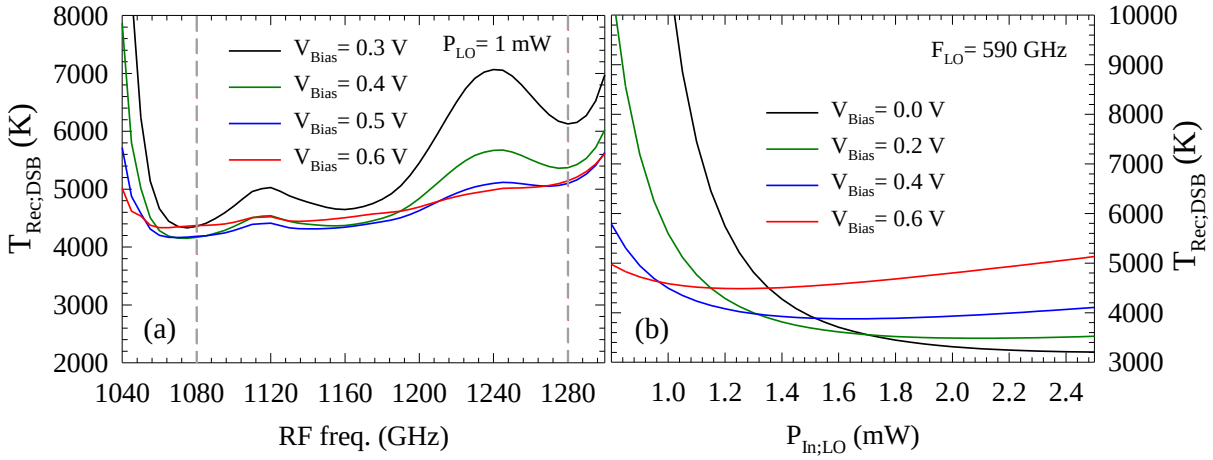

Fig. 6.23. ADS-HFSS results of the DSB noise temperature of the receiver $T_{Rec;DSB}$ at 5 GHz of IF signal using the STD model. Figure (a) shows the $T_{Rec;DSB}$ when sweeping the LO frequency signal and the bias signal at 1 mW of LO input power. Figure (b) shows the $T_{Rec;DSB}$ when sweeping the available LO input power and the dc bias at a fix LO frequency of 590 GHz. The simulations consider room temperature conditions.

The presence of the bias in the DSB noise temperature performed by the receiver clearly improves it and it is predicted from 0.5 V to 0.6 V to obtain the best performance at 1 mW of LO input power and requires around 2 mW of LO input power to obtain the best performance without biasing the diodes. It is interesting to note the influence that hot-electron noise can have in the performances presented in Fig. 6.23(b). It has been analyzed in [Crow87], [Thom03] and [Thom04], that the hot-electron noise usually appears when strongly pumping the diode cell and it increases the noise temperature of the receiver as the LO input power increases. We can therefore expect the optimal input power of our receiver, without biasing the diodes, to be around 1.8 mW of LO input power with some more DSB noise temperature. The optimal LO input power is reduced as the bias is increased, since the excited voltage signal by the LO signal in the diode cell enters in the flat band region of the I-V characteristic. The increment of the minimum DSB noise temperature, when increasing the bias, is associated to a smaller conversion efficiency of the diodes under that pumping condition.

It is important at this point to discuss again the impact of α parameter in the Schottky diode model of the C-V characteristic. It has been appreciated an important impact of the simulated α parameter in the PSBD model which defines the interaction of the I-V and C-V characteristic in the proximities of flat-band conditions. It modifies the slope of the minimum DSB noise temperature obtained in Fig. 6.23(a) and also the noise level. The higher the value of the parameter α in the STD model simulations, the higher the slope obtained in Fig.

6.23(a), the higher the required bias to minimize the noise temperature and the higher the minimum DSB noise temperature level. In fact, this design was optimized by considering a parameter α= 0.6 that predicts a very flat noise temperature performance of the biased receiver pumped with 1 mW of LO input power with a minimum DSB noise temperature around 3500 K. The results presented in Fig. 6.23 are obtained with α= 0.85 and the minimum DSB noise temperature is higher than 4000 K and it clearly enhances the IF generation at the low frequencies of the band. The only difference in the mixer performance when changing the α value is in the $L_{D;SSB}$ factor. It means that it is possible to enhance the conversion efficiency of the high frequencies of the mixer design using a high value of α parameter and vice versa. We recall that this model of the flat band conditions is extremely simple and the definition of α parameter is principally used to avoid the indetermination of the C-V characteristic at $V=V_B$ where $C(V_B)= \infty$. The author has observed a tendency of the fabricated chips of mixers to yield better results at the low frequencies of the band, which can be reproduced by high values of the α parameter together with the consideration of a RLC circuit, as will be discussed later. Regarding the predicted optimal bias, the impact of α parameter is quite important at this point since the predicted optimal bias when simulating a α= 0.6 is between 0.4 V to 0.45 V while it increase up to 0.5 V to 0.6 V when a α= 0.85 is considered.

6.4.6.2 The RLC Equivalent Circuit

The RLC circuit model to define the impedance of the epilayer of the PSBDs in series with the junction model is discussed in this subsection. The same value of total series resistance R_S= 86 Ω is simulated in this case, but this resistance will be distributed between the resistance R_{Int} included in the RLC circuit and the series resistance R_{Ext} in series with the RLC circuit. The simulated thermal noise is associated with the same value of thermal resistance considered in the previous sections (around half of the R_S= 86 Ω). The L and C values are calculated as indicated in [Gonz97], [Louh95] by using the series resistance R_{Int} that is involved in the RLC circuit. The DSB noise temperature obtained when considering a RLC circuit from $R_{Int}= 0 \cdot R_S$ to $R_{Int}= R_S$ has been plotted in Fig. 6.24(a) and the corresponding SSB conversion loss of the receiver has been plotted in Fig. 6.24(b).

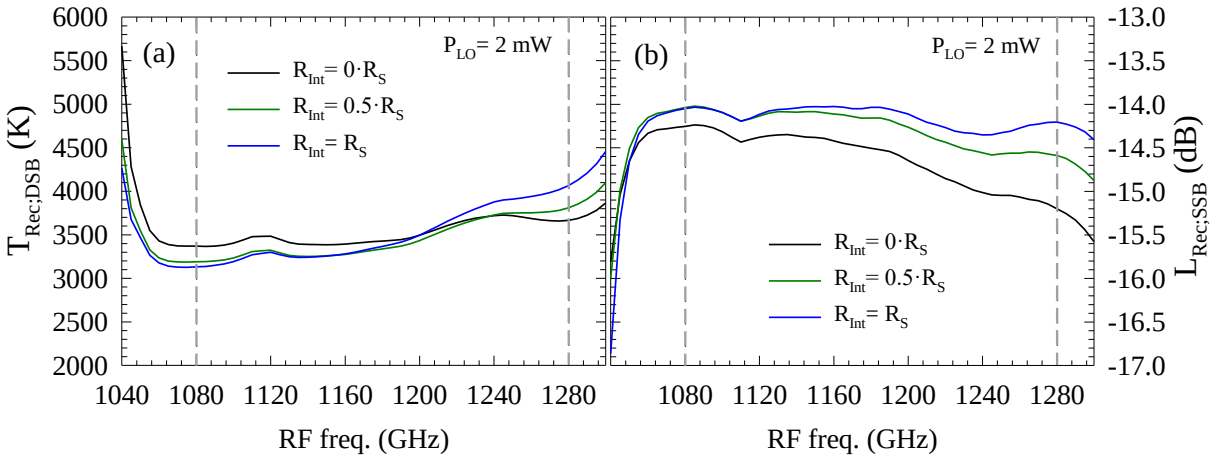

Fig. 6.24. ADS-HFSS results of the DSB noise temperature of the receiver $T_{Rec;DSB}$ at 5 GHz of IF signal using the STD model and a RLC series impedance. Figure (a) shows the $T_{Rec;DSB}$ when sweeping the considered resistance R_{Int} of the RLC circuit at 2 mW of LO input power and null bias. Figure (b) shows the $L_{Rec;SSB}$ in the equivalent conditions. The simulations consider room temperature conditions.

It is possible to view in Fig. 6.24 how the RLC circuit modifies the performances of the device. The L_{RF} factor decreases, the L_{LO} factor increases and the $L_{D,SSB}$ factor decreases when the R_{Int} contribution (with the calculated C_{Int} and L_{Int}) increases. The L_{RF} factor and the L_{LO} factor suffer only a small shift value along the frequency band, but it is the $L_{D,SSB}$ factor which is substantially modified. The $L_{D,SSB}$ factor difference is responsible for the performance modification in the tendency along the band indicated by Fig. 6.24(b). Regarding the noise temperature, it is not changed since the *CL* does not contribute any noise, but the distribution of the noise $T_{Rec;DSB}$ is notably modified along the frequency band due to the term $L_{Mix;DSB}{\cdot}T_{IF}$ in eq. 6.2. Observing the LO signal coupling and the extracted value of $T_{D;DSB}$, it has been concluded that very similar LO power values arrive into the diode cell and an almost equivalent $T_{D;DSB}$ is generated by the diode cell in spite of the changes in the L_{RF} and the L_{LO} factors. The black line in Fig. 6.24 represents a pure series resistance model used in Fig. 6.22 while the blue line represents pure RLC series impedance model (which is theoretically not possible). It is possible to conclude that the presence of the RLC circuit modifies the relationship, previously optimized with the pure series resistance model, between the LO and the RF signal to generate an IF signal along the frequency band. This means that the impedance matching of the diode cell along the band is changed by the RLC circuit and the efficiency of IF generation is shifted toward the low frequencies of the band. It is equivalent to the results obtained when changing the simulated α parameter in the STD model of the diode in the previous discussion. The modeling of the flat band conditions used to obtain the results of Fig. 6.24 is defined in this case by both the integrated α parameter for the C-V characteristic and an external RLC circuit simulated in series with the diode model. The conclusion is that the RLC circuit is able to affect more the general tendency along the frequency band due to its intrinsic dependence on the frequency, while α parameter induces an almost constant shift in the conversion efficiency along the band.

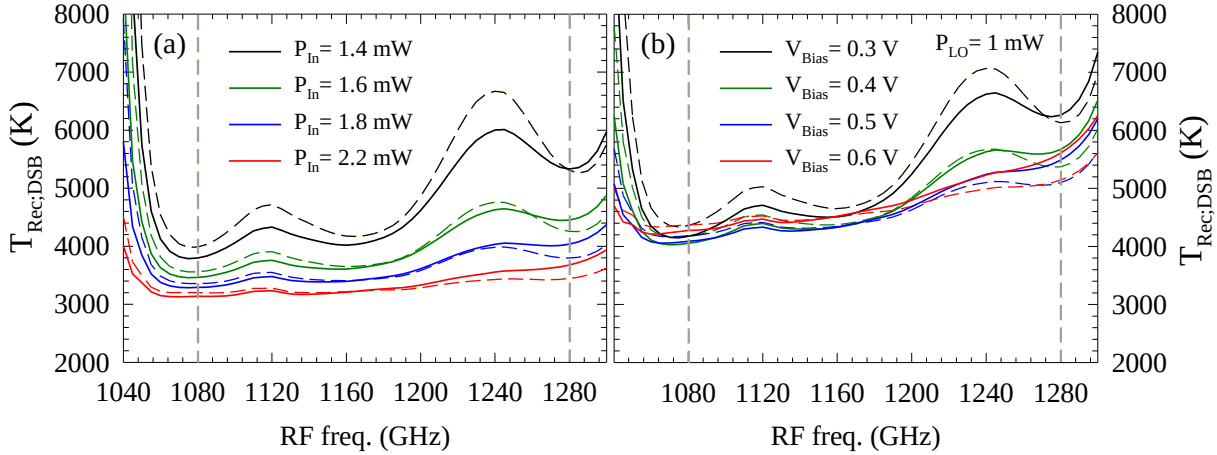

Fig. 6.25. ADS-HFSS results of the DSB noise temperature of the receiver $T_{Rec;DSB}$ at 5 GHz of IF signal using the STD model. Figure (a) shows the $T_{Rec;DSB}$ when sweeping the LO input power without biasing the diodes. The $T_{Rec;DSB}$ when sweeping the bias at 1 mW of LO input power is plotted in Figure (b). The results obtained with the RLC circuit (solid lines) and a pure series resistance (dashed lines) are compared. The simulations consider room temperature conditions.

The analysis carried out in Fig. 6.24 is now repeated using the RLC circuit when considering a R_{Int}= 0.55·R_S. The same α= 0.85 is considered in Fig. 6.25(a) when sweeping the LO input power from 1.4 mW to 2.2 mW without biasing the diodes. The equivalent study when sweeping the bias from 0 V to 0.6 V at 1 mW LO input power is presented in Fig. 6.25(b).

The comparison of the DSB noise temperature results, obtained between the case in which the RLC circuit (solid lines) and only the series resistance (dashed lines) have been included in the diode simulation, is accounted for in Fig. 6.25. The results obtained in Fig. 6.25(a) with the RLC circuit are not notably better in terms of global noise (as expected) but the minimum noise temperature at higher/smaller frequencies is higher/smaller than the case where only a constant series resistance is simulated. However, the most interesting result is the reduced predicted optimal bias when simulating the RLC circuit. The optimal bias is found between 0.4 V to 0.5 V in this case (~0.1 V lower than in the pure series resistance model) for 1 mW of LO input power. This means that the predicted optimal bias would be even lower if α parameter is reduced (it would also reduce the global noise due to an reduction of the $L_{D;DSB}$ factor). This effect is illustrated in Fig. 6.26, where the RLC circuit induces a lower DSB noise temperature at low LO input power than the case with a constant series resistance mode. It is possible to note that the red line already predicts a higher noise temperature for the simulated RLC circuit since the optimal bias has been exceeded.

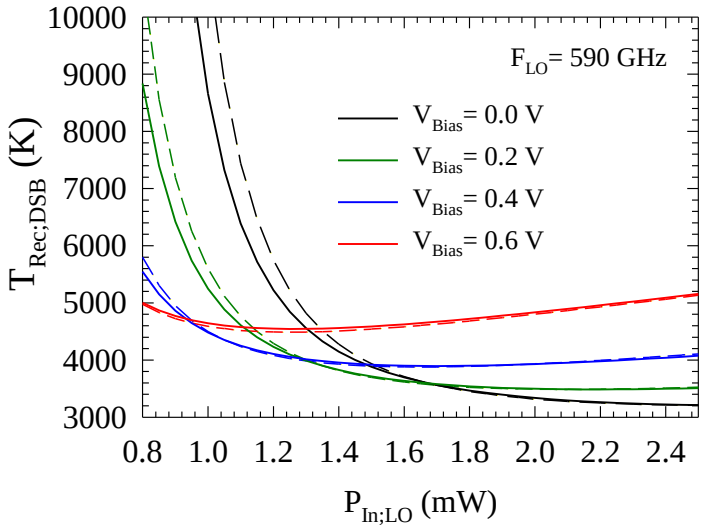

Fig. 6.26. The $T_{Rec;DSB}$ when sweeping the available LO input power and the DC bias at a fix LO frequency of 590 GHz considering the RLC circuit (solid lines) and pure series resistance (dashed lines). The simulations consider room temperature conditions.

It has been observed that the RLC circuit can be useful for future designs of frequency mixers since it can help to mitigate the overestimation of the performances at low frequencies at expenses of the higher frequencies. This RLC circuit doesn't help either in the predicted DSB noise temperature or the conversion loss of the receiver and it introduces an additional complexity during ADS-HFSS optimization of the device. However, the minimization of the DSB noise temperature along the band when including a RLC circuit can lead to a closer situation to the real PSBDs response.

6.4.7 Conclusions

The different considerations and concepts required to understand a frequency mixer device base in PSBDs have been discussed thoroughly in this section. The conversion loss concept and how it impacts the defined noiseless temperature of the receiver have been detailed in section 6.4.1 and 6.4.3. A theoretical technique that can be found in the bibliography to study the noise contribution of the diode cell of a frequency mixer in the final noise delivered into the IF port have been briefly discussed in section 6.4.2. The conversion loss concept has been

applied in section 6.4.4 in the ADS-HFSS simulations of the designed in-channel and out-channel mixer chips presented in section 6.2. The additional contribution to the DSB noise temperature introduced by the diode cell has been discussed in section 6.4.5, where the accuracy of the quantitative results presented in the different figures has been pointed out in accordance with the simulated models of the Schottky diode. The out-channel design has been concluded to be the more suitable candidate for the proposed 1.2 THz receiver for the SWI instrument. The impact of the bias in the performance of the mixer when reducing the LO input power to realistic values has been analyzed in section 6.4.6. The impact of an external RLC circuit in series with the junction model of the Schottky diodes and the α parameter in the definition of the C-V characteristic of the junction model, has also been discussed in this last section to determine the influence of each one in the Schottky diodes performance. α parameter has demonstrated to be critical in the predicted optimal bias of the mixer when fixing the simulated LO input power, while the RLC circuit has indicated that the dependence of diodes cell matching on the frequency, can be accounted for when including it in the optimization of the microelectronic circuit.

6.5 Experimental device

The ensemble of the experimental development of the 1.2 THz frequency mixer based on the out-channel design discussed in section 6.2 and 6.4, is presented in Fig. 6.27. The images of the fabricated mechanical block together with the image of the fabricated chips before releasing them from the wafer and the already mounted chip performs the ensemble of the fabrication process developed by LERMA-LPN-CNRS.

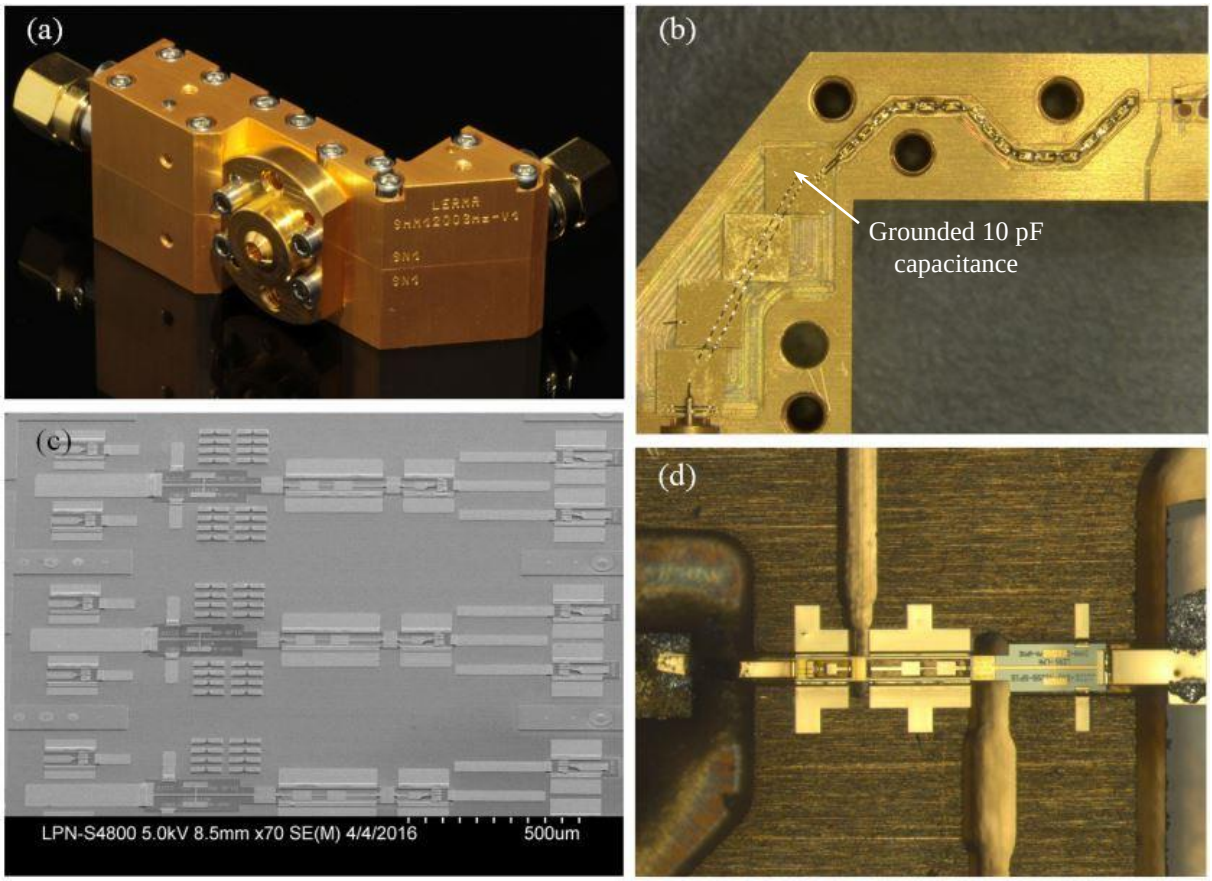

Fig. 6.27. Images (a) and (b) are the photographs of 1200GHz frequency mixer block fabricated by SAP-micro before assembly. (c) Photography of the MMIC chips of the out-channel 1200 GHz mixer design fabricated by LPN before releasing them from the wafer. (d) 1200 GHz MMIC mixer chip mounted in the mechanical block.

The mounted DC and IF circuits can be observed in Fig. 6.27(b), where the bonding of the non-grounded capacities leads the DC bias from the SMA connector to the diode cell. The IF signal generated by the diode cell can also propagates towards the DC circuit, but a grounded 10 pF capacity has been included in the DC circuit in parallel to the bonding cables in order to correctly ground the IF signal in the DC side. The image of the MMIC chips before release from the wafer corresponds to the second-generation chips of the 1.2 THz mixer design. It is possible to view in Fig. 6.27(c) some diode cell test structures placed in the space between the 1.2 THz mixer chips. The mounted chip in Fig. 6.27(d) corresponds to the first functional 1.2 THz mixer of the first generation.

6.5.1 I-V Characteristics of the Diodes

Experimental I-V characteristics of diodes can be obtained thanks to the separate IF and DC circuits defined in the MMIC chip. I-V characteristic in series configuration of the diodes can be obtained from the DC connector while the individual I-V characteristics can be obtained from the combination of the DC and the IF connectors. The I-V characteristic of one of the diodes can be individually characterized if a cero bias is fixed in the DC connector and the IF connector is used to bias the diode cell. The other diode can be similarly characterized fixing a cero bias in the IF connector and biasing from the DC one. A representative measurement of the I-V characteristic of one of the 1.2 THz MMIC mixer modules is presented in Fig. 6.28. The results correspond to a 0.18 μm^2 anode size instead of the nominal one defined at 0.2 μm^2.

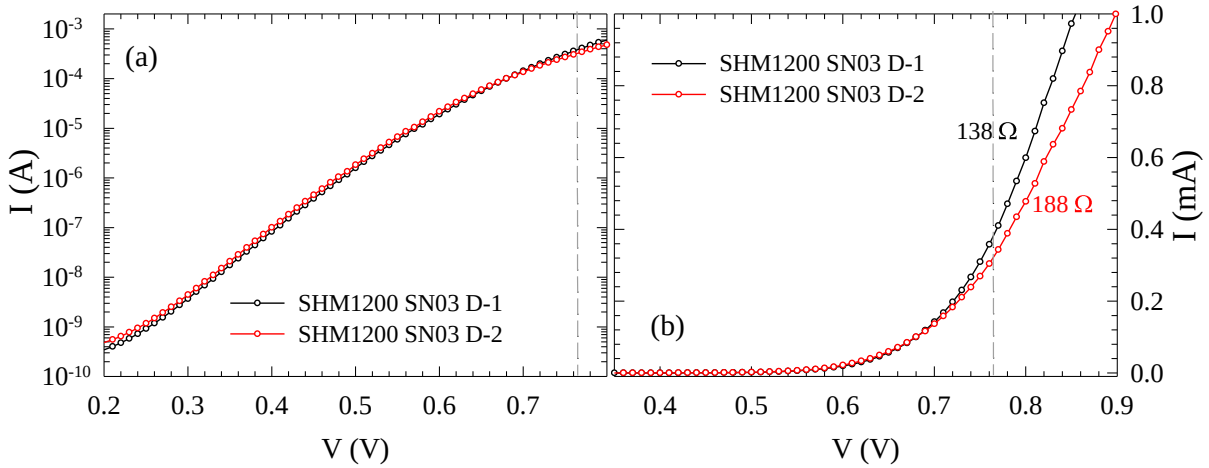

Fig. 6.28. I-V characteristics of the fabricated 1200 GHz mixer chip mounted in the SN03 block in (a) logarithmic and (b) linear representation. The I-V characteristics of each PSBD are compared.

It is possible to note a difference of the DC series resistance of each diode in Fig. 6.28(b). The indicated number is the value of the inverted slope of the linear part of the I-V characteristic after flat band. This difference will disturb the balance configuration of the diode cell and a certain degradation of the noise temperature performance will be associated.

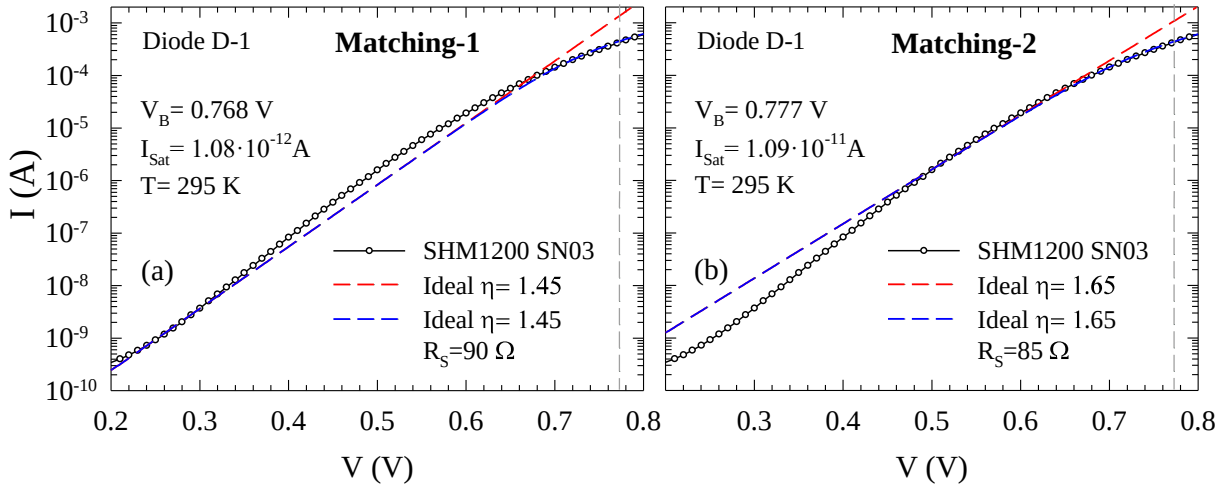

Fig. 6.29. I-V characteristics of diode one in a fabricated 1200 GHz mixer chip mounted in the SN03 block in logarithmic representation. The physical parameters of the diode are calculated by fitting the experimental results (black dots) with the analytical model (dashed blue line).

The experimental I-V characteristics are used to define the analytical simulation parameters of the PSBDs. However, there is a certain indetermination of the ideality factor and the DC series resistance using the exponential I-V model to fit these experimental results. The analytical fitting of the I-V experimental results have been carried out in Fig. 6.29, where two different matching of the I-V have been proposed. The matching-1 tries to fit the I-V characteristic at high currents (close of flat band) and low currents (few hundreds of millivolts), while the matching-2 enhances the fitting of the I-V characteristic above 0.5 V of DC bias. The matching-1 leads to a lower ideal factor and saturation current than the matching-2, but it does not fit correctly to most of the experimental points at bias between 0.4 V to 0.65 V. The extracted built-in voltage is similar in both cases. There is a deviation of the experimental I-V curve from the ideal exponential tendency associated to Schottky diodes, previously remarked in the bibliography [Koll86], that does not allow fitting the I-V characteristic as well as in previous devices. This deviation can be associated to defects in the Schottky anode fabrication due to the small anode size required for this application. A series resistance between 85 Ω to 90 Ω is found in Fig. 6.29, but the value obtained in Fig. 6.29(b) is more accurate since the current values are better reproduced in the proximities of flat band. This value is slightly smaller than expected for the nominal anode size (0.2 μm^2) proposed in section 6.4 because it is performed by a smaller anode (0.18 μm^2). The same analysis is carried out for the second diode and it is plotted in Fig. 6.30. The second diode presents the same deviation from the ideal exponential tendency and similar values of built-in voltage and saturation current than the diode one in Fig. 6.29. However, the required series resistance to fit the experimental measurements is much higher. A higher value of the series resistance in one of the diodes has been obtained in all functional modules that have been tested. The only one which performed similar series resistances was not functional in RF conditions. We do not have an explanation for this higher value.

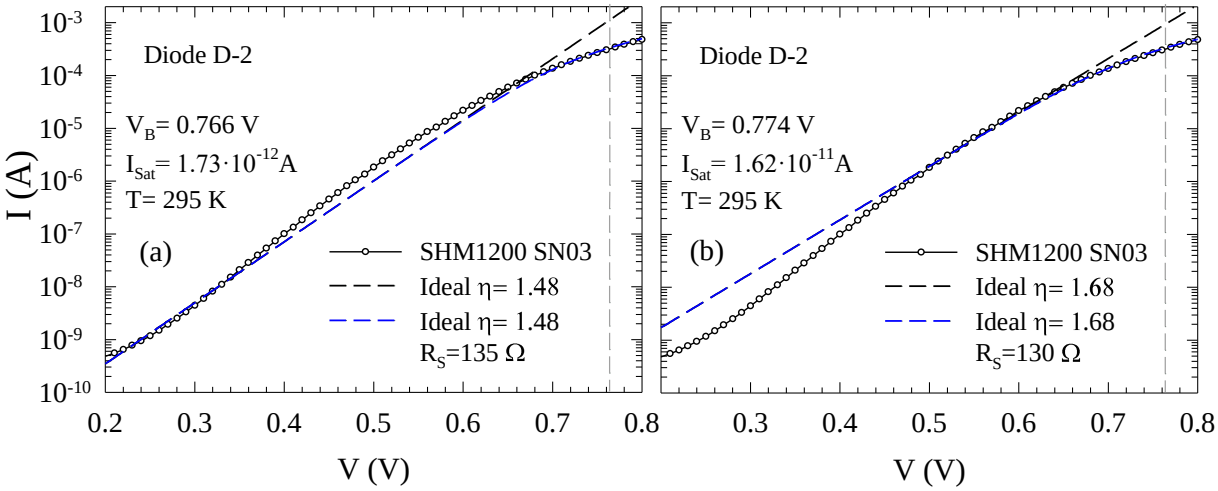

Fig. 6.30. I-V characteristics of diode two in a fabricated 1200 GHz mixer chip mounted in the SN03 block in logarithmic representation. The physical parameters of the diode are calculated by fitting the experimental results (black dots) with the analytical model (dashed blue line).

The high value of the series resistance of one of the diodes will dramatically increase the noise temperature of the receiver since the conversion efficiency of one diode cell will decrease, thus the noiseless temperature (eq. 6.18) of the receiver will increase. Additionally,

the noise temperature contribution of one of the diodes $T_{D;DSB}$ will also increase due to the higher thermal noise source. Regarding the different matching proposed in Figs. 6.30 and 6.29, the second matching is considered by this author to compare the experimental results with the simulations in the next section. This matching is considered to be closer of the reality since it fits better the high currents of the I-V characteristics where the diode response is more determined by the conduction current ($I_d(t)$) than from the diffusion current ($C(t)dV/dt$). This results in an ideality factor $\eta \approx 1.66$, a saturation current $I_{Sat} \approx 1.3 \cdot 10^{-11}$ A and a built-in voltage $V_B \approx 0.78$ V. The higher values of the ideality factor and the saturation current will induce a degraded response of the diodes compared with the nominal values used in section 6.4 and it will be even more degraded by the higher series resistance value of one diode. Regarding the impact of a different series resistance, additional frequency components are expected to be propagated out of the diode cell due to the quasi-balance conditions of the diodes.

6.5.2 The Y-factor for Experimental Measurement

This section is dedicated to briefly explain the main experimental considerations when measuring the noise temperature of the receiver from the Y-factor measurement [Kerr99]. The Y-factor of a frequency receiver can be obtained comparing the difference of output IF signal power given by the receiver when detecting two RF signal sources at different temperatures. The output power of the receiver is given by $P_{out}=G(P_R+P_{In})$, where G is the receiver gain, P_R is the equivalent input noise power of the receiver in band B and P_{In} is the input noise power in the receiver. The Y-factor experimentally measured is based on the definition given by eq. 6.22 in terms of the quotient of the measured IF output power delivered by the receiver when loading the RF port with two loads at different physical temperatures,

$$Y = \frac{P_R + P_{hot}}{P_R + P_{cold}} = \frac{T_{Rec} + T_{hot}}{T_{Rec} + T_{cold}} \quad , \tag{6.22}$$

where P_{hot} and P_{cold} are the input noise power delivered by the load (as black-body radiator) that can be calculated with the Rayleigh-Jeans law ($P=kT$) at the physical temperature of the load T_{hot} and T_{cold}, respectively. The Rayleigh-Jeans approximation is good enough in the frequency and temperature ranges used in the measurements of our receiver. The values T_{hot} and T_{cold} need to be corrected with the Callen and Welton law [Kerr99] if the frequency is tens of THz or the temperature is only few kelvins. The Y-factor from eq. 6.22 can be expressed in dB as the difference between the output power in dB delivered by the receiver loaded with a T_{hot} and T_{cold} black-body emission. The higher the Y-factor, the smaller the noise temperature of the receiver, as indicated in eq. 6.23,

$$T_{Rec} = \frac{T_{hot} - Y \cdot T_{cold}}{Y - 1} \quad . \tag{6.23}$$

It is important to be able to correct the DSB noise temperature of the receiver in accordance with the transmission losses of the RF signal from the RF source to the RF antenna of the receiver. It can be carried out by correcting the effective temperature of the hot and the cold source including an attenuator model. The effective temperature of a RF source at temperature T_S when an attenuator at temperature T_{att} is placed between the source and the receiver is given by,

$$T'_S = T_S \cdot t + (1 - t) \cdot T_{att} \quad , \tag{6.24}$$

where *t* is the transmission coefficient of the attenuator. The first term is associated to the transmitted RF radiation from the RF source while the second term is associated to the black body radiation emitted by the attenuator (equal to the absorbed radiation).

The eq. 6.24 can be applied to correct the DSB noise temperature of the receiver when accounting for the transmission losses of the RF signal in the air. The cold source at 77 K must be corrected using the eq. 23, where the attenuator is the air (with certain humidity) between the cold source and the receiver. The hot source needn't be corrected since the air is at the same temperature of the hot source.

6.5.3 RF Results of the 1.2 THz Receiver at 300 K

The experimental results obtained with a functional module of the 1.2 THz mixer are presented and discussed in this section. The scheme of the 1.2 THz receiver proposed for the SWI instrument is presented in Chapter 1 (Fig. 1.2), and the experimental test bench presented in Fig. 6.31 follows exactly that configuration.

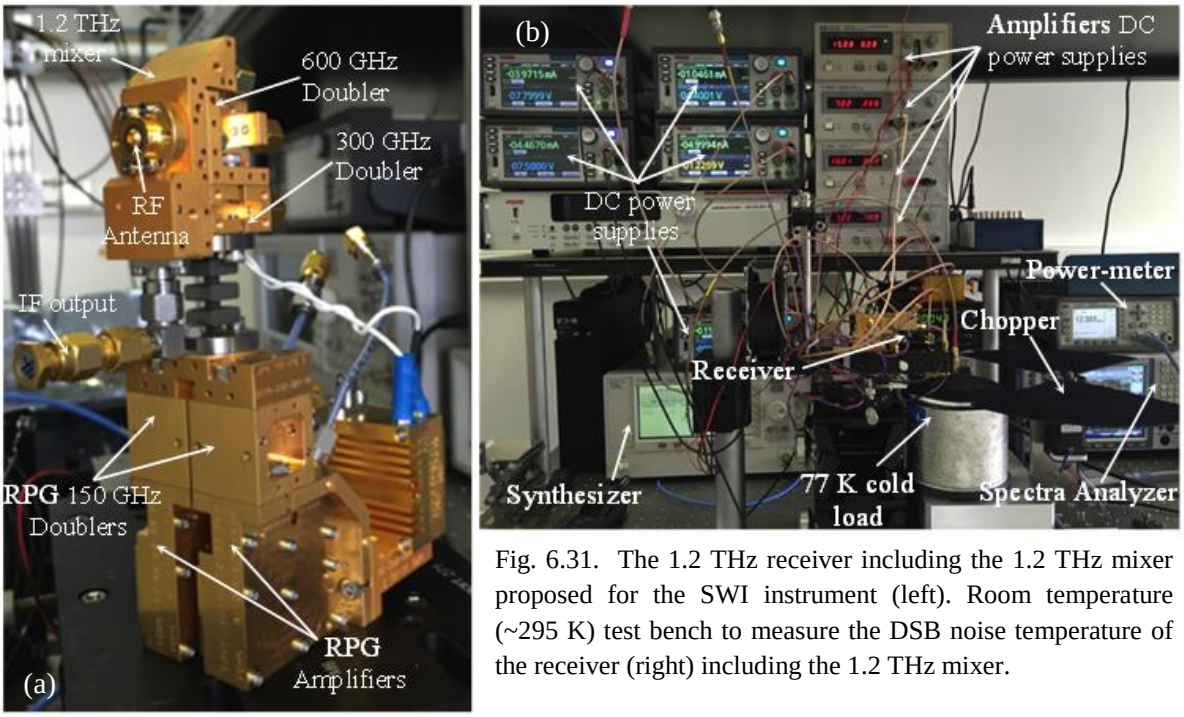

Fig. 6.31. The 1.2 THz receiver including the 1.2 THz mixer proposed for the SWI instrument (left). Room temperature (~295 K) test bench to measure the DSB noise temperature of the receiver (right) including the 1.2 THz mixer.

The full 1.2 THz receiver that includes the 1.2 THz mixer is presented in Fig. 6.31 (a). It is possible to see the RPG source which consists of a frequency tripler in E-band to pump a E-band booster amplifier. The next stage splits the power to pump two additional amplifiers that are used to separately pump two RPG 150 GHz frequency doublers. This source is able to deliver a combined power higher than 60 mW in the full required band (135 – 160 GHz) with maximum power around 80 mW in the center frequencies. A titanium waveguide section behaves as thermal break between the RPG source and the LERMAs receiver for the cryogenic measurements. The designed test bench for room temperature measurements is shown in Fig. 6.31(b), where 5 voltage sources for the doubler and mixer modules and four DC power supplies for the amplifiers are required to tune the different modules of the receiver. An initial frequency signal from 22.5 GHz to 26.67 GHz is generated by the Agilent E8257D synthesizer. The 1.2 THz mixer is now connected to the same configuration used in the measurements of the 600 GHz doubler in section 4.1.3. A 77.4 K liquid nitrogen is used as

a cold RF source and a chopper with thermal isolation is used as a hot RF source. The measurement of the noise temperature of the receiver from 4 GHz to 8 GHz of the IF signal is carried out automatically using the Labview software. The DSB noise temperature of the receiver over RF frequency is measured with an Agilent power-meter N1912 with E9300A power sensor during a constant exposition time of the hot and the cold sources in front of the RF antenna. The results obtained with four sets of measurements using that procedure allows calculating the average Y-factor at each LO frequency as indicated by eq. 6.22. The 1.2 THz mixer is pumped by the 600 GHz doubler presented in section 4.1. The optimal bias used by the RPG 150 GHz doubler and the 300 GHz doublers to obtain the results presented in section 3.2.4 are fixed for this experiment. The 600 GHz doubler is now biased to find the best performance of the receiver. Unfortunately, the 1.2 THz mixer couldn't be biased to mitigate the lack of LO power form the LO source. The reason was found several month later associated to the low noise amplifier (LNA) used to amplified the IF signal from 4-8 GHz. This is a Miteq LNA for room temperature measurements that presents 0.7 dB noise figure. It has been concluded that this amplifiers doesn't have an integrated series capacitor in the input. The lack of input capacitor in this LNA Miteq amplifier modifies the DC path defined for the diodes and the biasing is not possible. The raw measurements of the DSB noise temperature (black dotted line) of the 1.2 THz receiver using one of the 1.2 THz mixer modules are plotted in Fig. 6.32. The anode surface of the fabricated PSBDs in this functional 1.2 THz mixer chip was estimated in ~0.24 μm^2. It is possible to note a raw DSB noise temperature between 5000 – 6000 K in most of the band and 6000 – 7000 K between above 1250 GHz RF frequency. The raw DSB noise temperature of the receiver is the noise temperature directly measured without correcting the values in accordance with the air absorption, i.e., without considering that the RF signal emitted by the cold and hot sources has been partially absorbed by the air. The raw DSB noise temperature has therefore been obtained by using eq. 6.23 with the average Y-factor experimentally measured and considering a T_{cold}= 77.4 K and T_{hot}= 293 K.

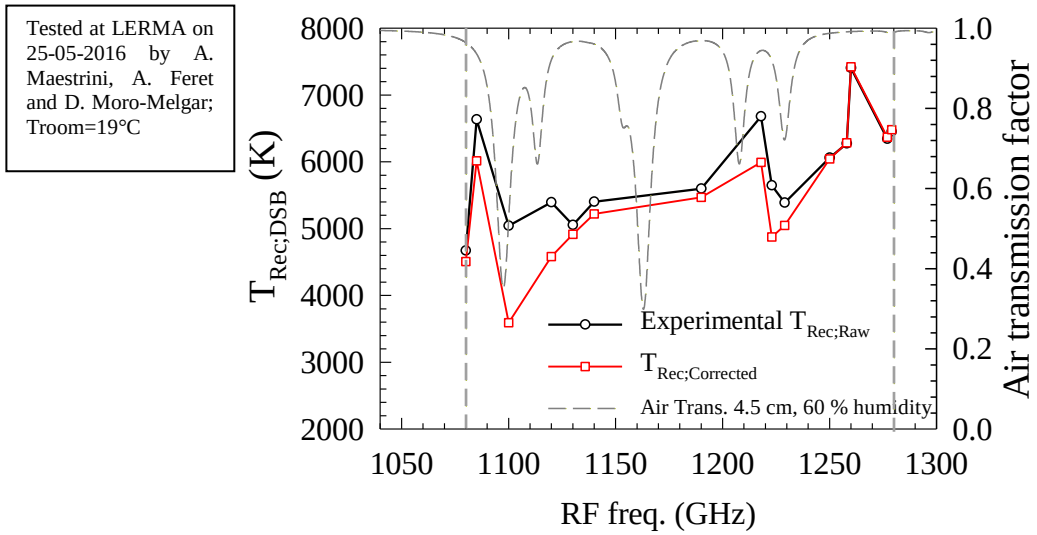

Fig. 6.32. Experimental DSB noise temperature (black line) measured with a power-meter along the RF frequency band at room temperature (~293 K) with the test bench indicated in Fig. 6.30. The corrected DSB noise temperature (red line) accounts for the air transmission coefficient (grey dashed line) of the USB and LSB frequencies in the 4-8 GHz IF frequency range.

The most important air compound that absorbs at these RF frequencies is the water vapor. The analytical expected absorption of the air in a 4.5 cm RF path from the cold source to the RF antenna and 60 % of humidity is plotted in Fig. 6.32 (grey dashed line). These transmission loses are calculated using the *am* Atmospheric model proposed in [Pain17]. It is

possible to see in Fig. 6.32 that there are important absorption lines of the water vapor at several frequencies of the considered range. The calculated air absorption allows correcting the raw DSB noise temperature value to obtain an approximation of the expected DSB noise temperature in vacuum conditions. It has to be calculated in accordance with the air transmission at the RF frequencies that contributes in the upper side band (USB) ($f=2\cdot f_{LO}-f_{IF}$) and the lower side band (LSB) ($f=2\cdot f_{LO}-f_{IF}$) of the IF signal between 4-8 GHz for each fixed RF frequency signal. This can be accomplished by modifying the effective T_{cold} value using eq. 6.24. The corrected DSB noise temperature of the 1.2 THz receiver is very similar to the raw DSB noise temperature except in the frequency points where there is a significant absorption by the air. A DSB noise temperature lower than 5500 K has been obtained in most of the band and some points are under 5000 K. The best performing frequency is found at 1100 GHz with a DSB noise temperature lower than 4500 K. The raw DSB noise temperature needs to be strongly corrected at this frequency in accordance with the air transmission (an average transmission factor 0.77 has been used at this frequency). The corrected DSB noise temperature above 1250 GHz is equivalent to the raw DSB noise temperature due to the high air transmission. A DSB noise temperature between 6000 – 7000 K is found at these frequencies.

An additional measurement has been carried out at 1100 GHz of RF frequency since it is the best frequency point obtained with this 1.2 THz receiver configuration. The Fig. 6.33 represents the average DSB noise temperature obtained by a Rhode and Schwarz FSV 40 GHz spectrum analyzer over the IF bandwidth (3–9 GHz) with a resolution of 10 MHz and with humidity of 60 %. The raw measurements are exhibited by the black line and the red lines represent the corrected value of DSB noise temperature, where the average of the USB and the LSB air transmission coefficient at each frequency of the IF band has been used to calculate the corrected T_{Cold} in eq. 6.23. The corrected DSB noise temperature shows an almost flat value over the IF frequency band under 4000 K.

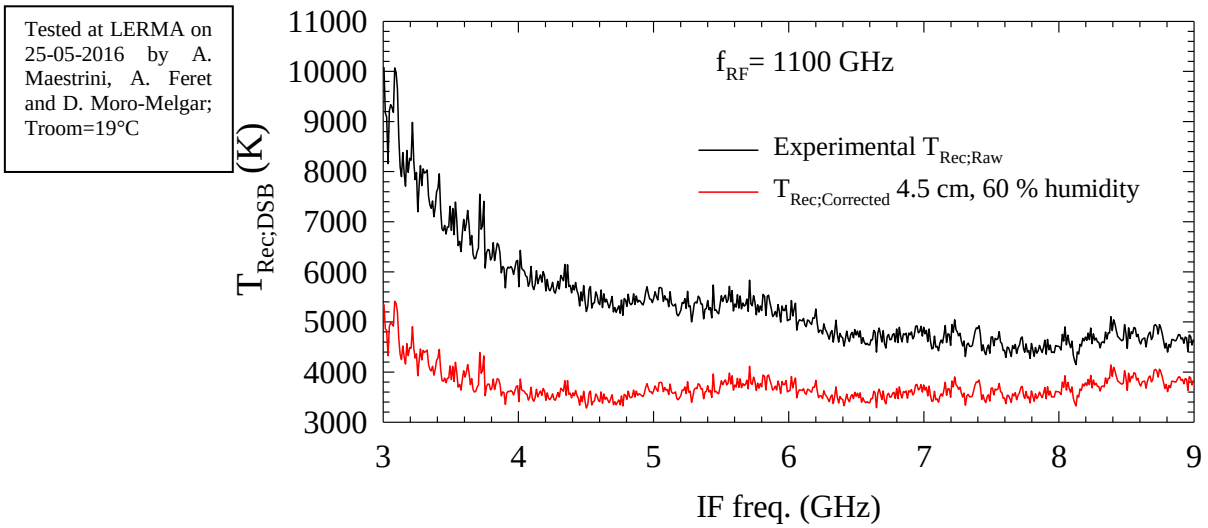

Fig. 6.33. Experimental DSB noise temperature (black line) measured with a spectrum analyses over the IF frequency band for 1100 GHz RF center frequency at room temperature (~293 K) with the test bench indicated in Fig. 6.30. The corrected DSB noise temperature (red line) accounts for the air transmission coefficient (grey dashed line) of the USB and LSB IF frequencies.

6.5.3.1 Experimental Observations

The measurements presented in Fig. 6.32 are quite delicate to carry out since several indeterminations can significantly modify these results. The most important one is the unknown LO input power which is supposed to be insufficient at several frequencies in

accordance with the experimental output power delivered by the 600 GHz doubler (section 4.1.3). This is the reason why a biasable mixer was developed from the beginning to mitigate the impact of a low LO input power in the 1.2 THz mixer. However, the bias of the 1.2 THz mixer has been found to be inoperative due to the lack of a input capacitor in the Miteq LNA. The bias presents a negative impact on the noise temperature since the input impedance of the amplifier induces the unbalance of the antiparallel diodes. However, additional noise introduced by the DC circuit when biasing the diodes has been considered as other probable reason for this experimental observation. Regarding the DSB noise temperature value along the band, it varies from 3600 K at 1100 GHz RF frequency to 7400 K at 1260 GHz RF frequency. The very high 7400 K DSB noise temperature value at 1260 GHz is in contrast to the 6200 K noise temperature at 1258 K. It is the similar case observed at 1085 GHz RF frequency where a DSB noise temperature of 6000 K is obtained while it is 4500 K at 1080 GHz and 3600 at 1100 GHz. These results can be explained in accordance with a lack of LO power at some frequencies due to the standing waves generated between the 600 GHz doubler and the 1.2 THz mixer. We recall that around a 40-50 % of the LO power is reflected in accordance with Fig. 6.19. This means that the reflected signal in the 1.2 THz mixer will react with the previous multiplication stage. It is impossible to determine in practice the effective LO input power in the experimental 1.2 THz mixer since the 600 GHz doubler results obtained in section 4.1.3 were already significantly modified by the standing waves, as discussed in section 4.1.4. This means that the LO power delivered by the 600 GHz in Fig. 4.6 is also modified by the standing waves generated when connecting the 1.2 THz mixer. It can explain the lack of LO power at certain frequencies while some GHz up or down there is more available power. Additionally, the unexpected challenge presented by the bias does not allow a clear identification of the lack of LO power.

It is possible to conclude that an increment of the effective LO input power in the 1.2 THz mixer will directly improve some of the points presented in Fig. 6.32. The point where there is a lack of LO power can also be improved if the experimental challenge of the bias circuit is addressed. This are the reasons why a redesigned 600 GHz four-anodes doubler has been proposed by this author, which is expected to be able to correctly pump the 1.2 THz mixer in most of the frequency even if no bias is used to tune the mixer.

6.5.4 RF Results of the 1.2 THz Receiver at 160 K

The receiver previously presented measured at room temperature has been measured now at cryogenic temperatures using a cryostat. A cryogenic test bench has been designed by the LERMAs engineer Alex Féret to correctly cool down the different parts of the receiver. The montage of the receiver presented in Fig. 6.31(a) was required to be modified in this experiment due to the limited room inside the cryostat. The E-band booster amplifier indicated in the 1.2 THz receiver scheme in Fig. 1.2 was removed to make room for the E-band RPG tripler inside the cryostat. A reduction of available LO power is expected due to this modification. However, no precise measurements of this modification on the available power were carried out at that moment. A different LNA is used for cryogenic temperature measurements of the receiver at LERMA. The origin of inoperative mixer-bias was not determined yet at this moment, thus the mixer-bias was not connected for these

measurements, as observed in Fig. 6.34(a). However, the LNA used for cryogenic measurements has an integrated input capacitor that would be found several months later. The dedicated montage is shown in Fig. 6.34(a) which is cooled down inside the cryostat shown in Fig. 6.34(b). The full receiver has been cooled down inside the cryostat while the RPG DM driver chain remains at higher temperatures using two separated plates. The LERMAs receiver and the RPG source are thermally isolated by the titanium waveguide section indicated in Fig. 6.31(a). The measurements are carried out in vacuum conditions inside the cryostat, thus the cryostat window and an optical mirror placed in the montage allow the transmission of the signal into the RF horn of the receiver. The cryostat windows consist of a 2 mm dielectric material with one or several λ/4 anti-reflection layers that allow improving the window transmission. The experiment was carried out at 21 Celsius degrees room temperature and a 35 % of humidity while the temperature inside the cryostat was fixed at ~160 K. The cold and the hot sources are shown to the 1.2 THz receiver in regular time steps to automatically generate an overage measurement of the Y-factor of the receiver at each considered frequency.

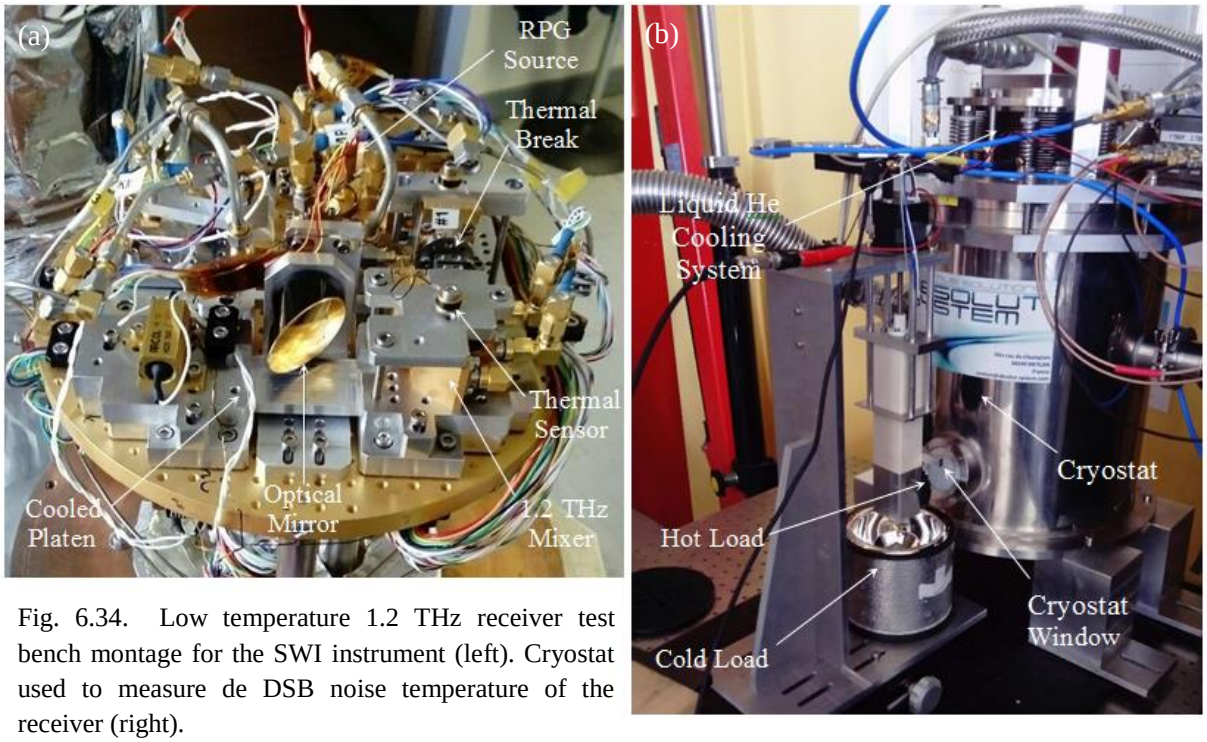

Fig. 6.34. Low temperature 1.2 THz receiver test bench montage for the SWI instrument (left). Cryostat used to measure de DSB noise temperature of the receiver (right).

6.5.4.1 Preliminary experimental results at 160 K

The transmission coefficient along the frequency band in the air (grey dashed line) (with 35 % humidity and 5.5 cm of distance between the cold source and the cryostat window), the cryostat window (blue dashed line) and the total transmission coefficient (black dashed line) are plotted in Fig. 6.35. The raw DSB noise temperature measured in these laboratory conditions at 160 K is provided by the black dotted line, while the corrected value of the DSB noise temperature is provided by the red dotted line in accordance with the transmission losses in the air and the cryostat window. The calculated absorption allows correcting the raw DSB noise temperature value to obtain an approximation of the expected DSB noise

temperature in vacuum conditions without the cryostat window. The correction factor has to be calculated in accordance with the average transmission coefficient at the RF frequencies that contributes in the USB ($f=2\cdot f_{LO}-f_{IF}$) and the LSB ($f=2\cdot f_{LO}-f_{IF}$) of the IF signal between 4-8 GHz for each fixed RF frequency signal. This can be accomplished by modifying the effective T_{cold} value using eq. 6.24.

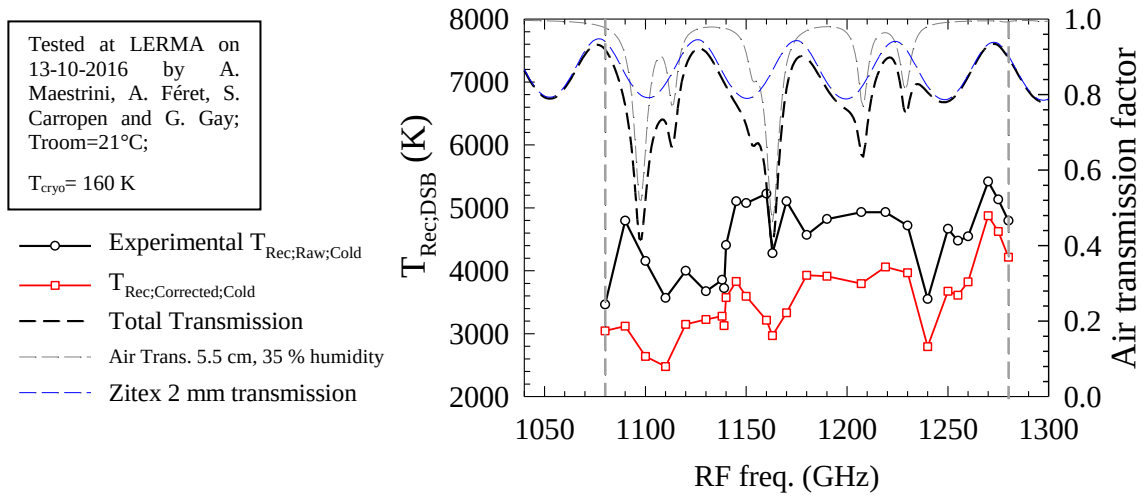

Fig. 6.35. Experimental DSB noise temperature (black line) measured with a power-meter along the RF frequency band at cryogen temperature (~160 K) with the test bench indicated in Fig. 6.31. The corrected DSB noise temperature (red line) accounts for the air (grey dashed line) and the cryostat window transmission coefficient (blue dashed line) of the USB and LSB frequencies in the 4-8 GHz IF frequency range.

The larger number of points that have been measured at cryogen temperatures can be associated to a higher LO power available to pump the 1.2 THz mixer. In fact, the delivered LO power by the 600 GHz doubler needs to be attenuated at several frequency points of the band to avoid the over-pumping of the mixer. This increment of the available LO power also allows obtaining a performance of the 1.2 THz mixer closer of the optimal one along the band despite the mixer-bias was not used for these measurements. Raw measurements of the DSB noise temperature vary between 3500-5000 K over the band. A reduced DSB noise temperature between 2500-4000 K has been obtained when accounting for the correction associated to the transmission losses. Although the best performance is not achieved with this first functional receiver, these results fulfill the sensibility and bandwidth specifications of the project that proposed less than 4000 K at 120 K between 1080-1280 GHz. The spectral line of the methane placed at 1256 GHz is also demonstrated by this first prototype.

6.6 Comparison with ADS-HFSS Individual Simulations

The analysis carried out in subsection 6.4.5 is now repeated in this section when considering the experimental deviation of the I-V characteristics observed in Figs. 6.28 and 6.29. The RLC circuit is now simulated as indicated in subsection 6.4.5. Regarding the definition of the I-V characteristic, an ideality factor $\eta \approx 1.66$ and a built-in voltage $V_B \approx 0.78$ V are employed in any simulation carried out in this section. These two parameters define the saturation current density $J_{Sat} = 61.76$ A/m^2 which is based on the results obtained in section 6.5.1. The anode surface of the PSBDs in the functional chip that performed the results presented in section 6.5.3 had an anode size ~0.24 μm^2. These data allows calculating an estimated $I_{Sat} = 1.47 \cdot 10^{-11}$ A and a junction capacitance $C_{j0} = 0.589$ fF in accordance with the model presented in Chapter 2. These are the values used to define the C-V characteristic and the I-V characteristic of the Schottky junction. Regarding the series resistance, the nominal total series resistance is estimated in $R_S = 75.2$ Ω that will be distributed between the internal R_{Int} and external R_{ext} series resistances of the RLC impedance model. The total series resistance of one of the diodes is now increased in the same proportion observed between the series resistances of the experimental chip analyzed in section 6.5.1. This means that one of the diodes is simulated with $R_{S;1} = 75.2$ Ω and the other one is simulated with $R_{S;2} = 115$ Ω. It is considered that $R_{Ext;i} \approx 0.45 \cdot R_{S;i}$ and its thermal noise contribution is enable in ADS simulations while $R_{Int;i} = R_{S;I} - R_{Ext;I}$ and its thermal noise contribution is disable. The results obtained with the ADS-HFSS simulations of the 1.2 THz receiver when sweeping the LO input power without biasing the diodes are plotted in Fig. 6.36. The simulations are carried out at room temperature (T~300 K). The simulation results obtained when considering the nominal simulation parameters of the PSBDs model (dashed lines), the new simulation parameters based on the experimental I-V analysis presented in section 6.5.1 (solid lines) and the experimental results discussed in section 6.5.3 are compared in Fig. 6.31.

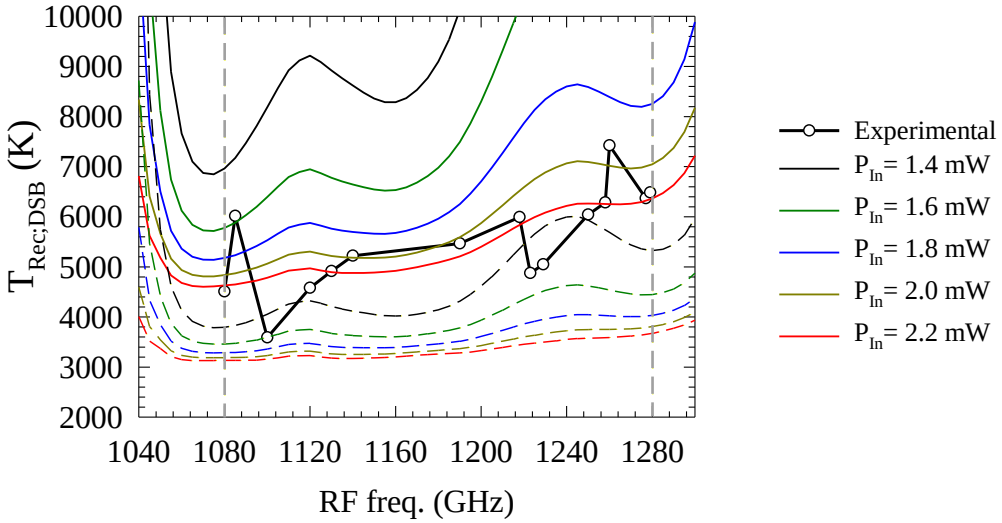

Fig. 6.36. The black dotted line is the experimental DSB noise temperature results of the 1.2 THz receiver. The DSB noise temperature simulation results obtained in the ADS-HFSS test bench of the 1.2 THz mixer are compared when considering the simulation parameters with the experimental analysis in section 6.5.1 (solid lines) and the nominal parameters used in section 6.4.5 and 6.4.6 (dashed lines).

It is possible to recognize the impact of the simulation parameters of the PSBD model in the global performances of the receiver. There is a difference higher than 1500 K at low

frequencies of the band and higher than 2700 K at high frequencies of the band between the results obtained with the expected nominal simulation parameters (dashed lines) and the new set of parameters based on the experimental DC I-V characteristics (solid lines). It is possible to note an increment in the slope of the DSB noise temperature along the frequency band that can be mainly associated to the increment of the anode size with respect to the nominal one. It is difficult to say if the new set of parameters allows a more suitable prediction of the experimental results, due to the incertitude in the DSB noise temperature calculation with our simple model. However, it is possible to affirm that the average experimental DSB noise temperature can be reduced between 1000 K and 2000 K along the band, in accordance with these simulations, if the experimental PSBDs physical properties are improved. The oversized series resistance presented by one of the diodes in all functional second generation chips of the 1.2 THz mixer and the high ideality factor are associated to the fabrication process. Previous PSBD devices used in the 600 GHz mixer presented in chapter 4, have performed a correct exponential behavior though its small anode surface. This indicates that better physical properties of the PSBDs for the 1.2 THz mixer can be achieved by the LPN in future fabrication runs.

The impact of the bias in the DSB noise temperature of the receiver when fixing the LO input power at 1 mW along the frequency band is analyzed in Fig. 6.37(a), and its impact when pumping at different LO input power for 590 GHz of LO frequency is analyzed in Fig. 6.37(b). These results (solid lines) are compared one again with the results obtained with the nominal set of parameters of the PSBDs (dashed lines). This comparison allows us to understand the global impact of the new simulation parameters.

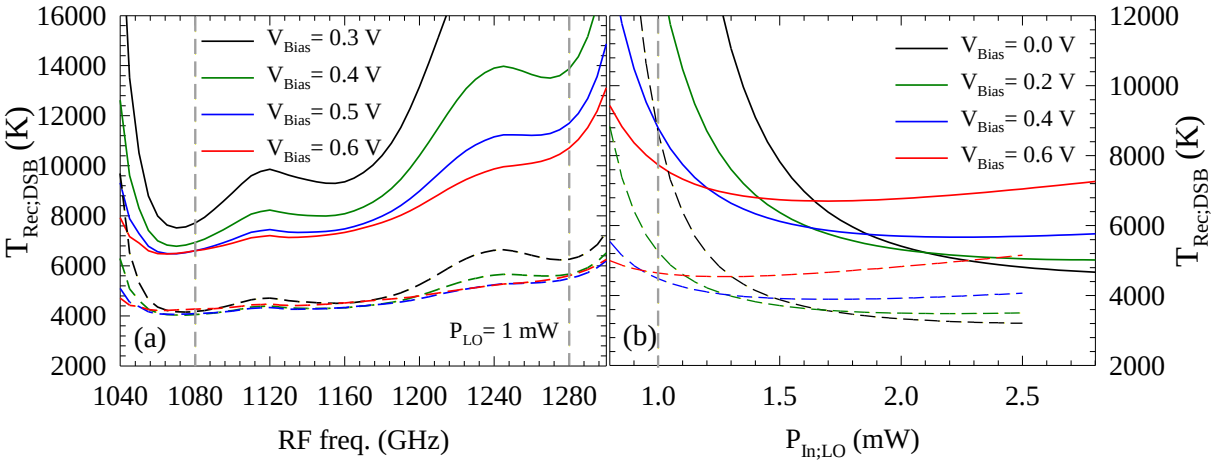

Fig. 6.37. DSB noise temperature simulated along the band (a) when pumping the 1.2 THz mixer with 1 mW of LO input power at different mixer-bias. DSB noise temperature simulated when sweeping the available LO input power (b) at 590 GHz LO frequency and different mixer-bias. The ADS-HFSS results obtained with the nominal physical parameters of the PSBDs (dashed lines) and the parameters based on the experimental I-V characteristics (solid lines) in section 6.5.1, are compared here.

The DSB noise temperature of the receiver when pumping with only 1 mW of LO power is expected to increase more than 2500 K at low frequencies and more than 5000 K at high frequencies even if the bias is optimized. Additionally, the optimum bias is increased for any LO input power considered in the simulation in accordance with Fig. 6.37(b). This means that the required LO input power and bias to get the optimal performance of the receiver have

increased with respect to the nominal case discussed in section 6.4. The conversion loss factors L_{RF}, L_{LO}, L_{IF} and $L_{D;DSB}$ have been analyzed and it has been confirmed that there is no change in the diode cell L_{RF}, L_{LO} and L_{IF} factors, but a different value for each diode of the diode cell is found, i.e., the diode with a higher resistance has a higher L_{RF}, L_{LO} and L_{IF} factors than the other diode but the average is the same obtained in section 6.4.4. This means that the DSB noiseless temperature (eq. 6.18) of the receiver does not dramatically change. A different $L_{D;DSB}$ factor is found once again for each diode since a different LO and RF input power is coupled in each one of them. The diode with a higher series resistance has a higher $L_{D;DSB}$ factor than the other diode, as expected, but the average $L_{D;DSB}$ factor calculated for the diode cell is also higher than the nominal one found in section 6.5.5. This is due to the increased ideality factor of the diode cell and the increased series resistance of one diode, which reduces even more the conversion efficiency of the RF into the IF. It is possible to conclude that all the additional noise temperature found in Figs. 6.36 and 6.37 comes from the increment of the $L_{D;DSB}$ factor. This is due to the higher ideality factor and series resistance of the diode cell, especially from one of the diodes that presents an even higher series resistance. This results in an general increment of the noise temperature $T_{D;DSB}$ (eq. 6.19) due to the higher noise power delivered to the IF port by the diode cell.

Regarding the comparison with the experimental results, higher bias and LO input power has been found necessary in this section to get the optimal performance of the receiver. In fact, much higher experimental DSB noise temperature than the obtained one in section 6.5 would be expected in accordance with these results. The expected LO input power from the experimental 600 GHz doubler (section 4.1.3) is between 1 mW to 1.8 mW in most of the band (lower in the edges) and the experimental 1.2 THz mixer bias is not used in most of the points presented in section 6.5.3. This means that the experimental behavior of the experimental 1.2 THz receiver does not match with the individual simulated behavior in the ADS-HFSS of the 1.2 THz mixer.

6.7 Simultaneous Simulation of the 600 GHz Doubler and the 1.2 THz Mixer

The interaction between the 600 GHz doubler and the 1.2 THz mixer developed by LERMA is studied in this section. The discrepancies between the predicted behavior of the 1.2 THz mixer simulated in the ADS-HFSS test bench and the experimental results, discussed in section 6.6, have led this author to hypothesize additional phenomena required to fully understand the assembly of the instrument. A significant interaction between the 300 GHz power-combined doubler and the 600 GHz doubler was pointed out in section 4.1.5, leading to satisfactory comparisons with the experimental results. The same idea is now applied to the interaction between the 600 GHz doubler and the 1.2 THz mixer since a higher interaction with the standing waves is expected now. The ADS-HFSS test bench used in section 4.1 to simulate the 600 GHz 2 anodes doubler is now used to pump the defined ADS-HFSS test bench of the 1.2 THz mixer used in section 6.6. The real dimensions of both mechanical blocks have been taken into account to correctly define the electrical path between the modules. Additional S-parameters simulations have been required to correctly define the interaction between both stages. It is first necessary to include the impact of additional harmonics of the 600 GHz doubler on the interaction between both stages. The third (~900 GHz) and fourth (~1200 GHz) harmonics of the 600 GHz doubler have been included in the simulation. An expanded simulation of the RF range for the 1.2 THz mixer has been required to take into account not only the RF input signal from the RF antenna, but also the fourth LO input harmonic generated by the 600 GHz doubler diode cell, which can potentially interact with the second harmonic generated by the 1.2 THz mixer diode cell. The simulation of the 1.2 THz mixer pumped by the third harmonic generated by the 600 GHz doubler diode cell has been also included to take into account its influence in the final frequency response of the 1.2 THz mixer. The simulation parameters of the 600 GHz doubler diodes are the same used in section 4.1.4 and the parameters used for the 1.2 THz mixer in section 6.6.

The most important results are presented in Fig. 6.38 and then the origin of the phenomena is discussed. The study carried out in Fig. 6.37(b) is now repeated when connecting the 600 GHz doubler to the 1.2 THz mixer. The DSB noise temperature of the receiver when the 600 GHz doubler is connected to the 1.2 THz mixer (solid lines) is compared with the individual simulations of the 1.2 THz mixer (dashed lines) carried out in the previous section. The bias of the 600 GHz doubler is fixed in this analysis and its simulated input power is defined by a one-tone power source at 295 GHz. The input power in the 600 GHz doubler has been swept to deliver an output power of the doubler between 0.8 mW and 2.2 mW. The bias point of the 600 GHz doubler diode cell has no influence on the results obtained in Fig. 6.38. The delivered power of the 600 GHz doubler at 590 GHz is measured at the point where the 600 GHz doubler mechanical block is connected to the 1.2 THz mixer block. The measured power is defined as the effective LO input power that pumps the 1.2 THz mixer. This effective LO input power is the result of the interaction between the 600 GHz doubler and the 1.2 THz mixer. The DSB noise temperature of the receiver in Fig. 6.38 has been plotted with respect the effective LO input power that pumps the simulated 1.2 THz mixer. The DSB noise temperature obtained with individual simulations of the 1.2 THz mixer has been compared to

the LO input power directly defined by a one-tone power source element of ADS. The same analysis has been carried out at different bias of the 1.2 THz mixer diodes.

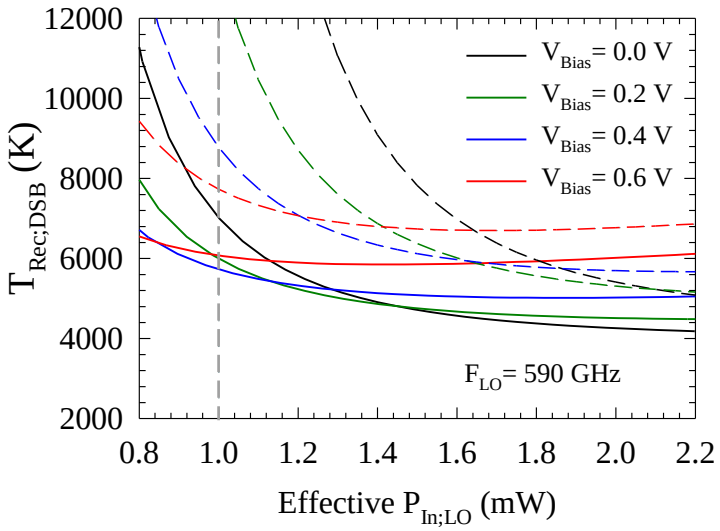

Fig. 6.38. DSB noise temperature of the receiver simulated with individual simulations of the 1.2 THz mixer (dashed lines) and simultaneous simulations of the 600 GHz doubler connected to the 1.2 THz mixer (solid lines). It has been represented with respect to the effective LO input power at 590 GHz for the 1.2 THz mixer from 0.8 mW to 2.2 mW. Different DC biases have been fixed in each case to compare the results. The simulations consider room temperature conditions.

A significant interaction between the 600 GHz doubler and the 1.2 THz mixer can be seen in the simulated DSB noise temperature of the receiver. The DSB noise temperature of the simultaneous simulation of the 600 GHz doubler and the 1.2 THz mixer shows a smaller value for an equivalent LO input power used to pump the 1.2 THz mixer. A ~1100 K DSB noise temperature reduction can be observed at 2 mW of effective LO input power between the minimum DSB noise temperature performed by the individual and the simultaneous simulations. A ~2000 K DSB noise temperature reduction can be observed at 1 mW of LO input power between the minimum DSB noise temperature performed by the individual and the simultaneous simulations. Additionally, the minimum value obtained in each case for each specific effective LO input power is obtained at lower optimal bias in the simultaneous simulations. The most important impact is observed at low effective LO input power values, where the simultaneous simulation of the 600 GHz doubler and the 1.2 THz mixer predicts 7000 K of DSB noise temperature even without any bias while the individual simulations of the 1.2 THz mixer predicts more than 30000 K. These simulation results explain the experimental results observed with functional 1.2 THz receivers that work even without biasing the diodes. It has been demonstrated that the full explanation of the receiver behavior cannot be predicted by individual simulations of the mixer due to the influence of the standing waves in the LO chain.

It is necessary to discuss at this point some observations obtained during the definition of the ADS-HFSS test bench accounting for the 600 GHz doubler and the 1.2 THz mixer. The simulation of the interaction between the fourth harmonic generated by the 600 GHz doubler diode cell and the 1.2 THz mixer has been found to be absolutely negligible. The effective LO input power at the fourth harmonic generated by the 600 GHz doubler is around 1 nW and the

presence of the RF filter between the LO antenna and the diode cell of the 1.2 THz mixer prevents the fourth harmonic of the 600 GHz doubler to reach the 1.2 THz mixer diode cell. However, a certain impact of the simulated third harmonic generated by the 600 GHz doubler in its own frequency response has been found. This impact has been only found in the final effective LO input power delivered to the 1.2 THz mixer when strongly pumping the 600 GHz doubler. No influence has been found when connecting this third harmonic with the simulated 1.2 THz mixer at that frequency. This means that the origin of the additional phenomena that significantly modifies the predicted DSB noise temperature in Fig. 6.38 is entirely associated with the interaction of the 600 GHz doubler and the 1.2 THz mixer at the LO frequencies (540 – 640 GHz). The only additional frequency simulation that has demonstrated any influence is the third harmonic generated by the 600 GHz doubler. The third harmonic has no impact on the 1.2 THz mixer diode cell response but it can slightly modify the predicted effective LO input power that pumps the 1.2 THz mixer. This author found that the simulation of the third harmonic of the doubler slightly reduces the predicted output power when over-pumping the doubler but it has no impact at reasonable pumping values. Once it is clear that the interaction between the 600 GHz doubler and the 1.2 THz mixer is fully determined by the LO signal around 600 GHz it is possible to focus the analysis on that frequency range. The LO and RF coupling efficiency in the diode cell of the 1.2 THz mixer when simultaneously simulating the 600 GHz doubler (solid lines) and when individually simulating the 1.2 THz mixer (dashed lines) are plotted in Fig. 6.39.

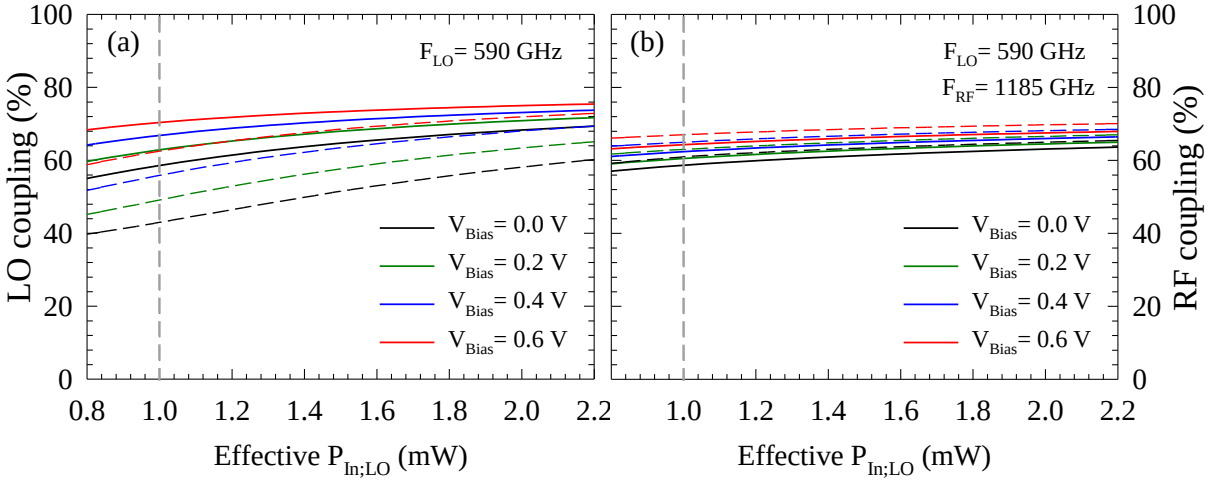

Fig. 6.39. LO (a) and RF (b) coupling efficiency of the 1.2 THz mixer diode cell when considering individual simulations of the 1.2 THz mixer (dashed lines) and simultaneous simulations of the 600 GHz doubler connected to the 1.2 THz mixer (solid lines). It has been represented with respect to the effective LO input power at 590 GHz for the 1.2 THz mixer from 0.8 mW to 2.2 mW. Different DC biases of the 1.2 THz mixer have been fixed in each case to compare the results. The simulations consider room temperature conditions.

It is possible to recognize a higher LO coupling efficiency of the 1.2 THz mixer diode cell predicted by the simultaneous simulations, especially when no bias is considered. Simultaneous simulations also indicate a reduced impact of the bias in the LO coupling efficiency that goes from a 58.6 % at 1 mW without bias to 70 % when biasing at 0.6 V, while the individual simulations predicts a variation from 42.7 % at cero bias to 63 % at 0.6 V. Regarding the RF coupling efficiency, small differences are obtained by individual and simultaneous simulation where the individual simulations of the RF coupling efficiency

predicts an almost constant 3 % additional coupled RF power along the band. The different RF coupling can be associated to the different LO coupled power, between individual and simultaneous simulations, that modifies the impedance matching of the RF signal.

It is possible to conclude that the interaction between the 600 GHz doubler and the 1.2 THz mixer induces a better LO coupling efficiency that explains the much improved performances of the receiver at low LO input power values. The next two subsections are dedicated to analyzing the predicted performances of the 1.2 THz receiver along the band when simulating the 600 GHz two anodes doubler and also included are the previsions when considering the 600 GHz four anodes doubler presented in section 4.2.

6.7.1 Simultaneous Simulations with the 600 GHz two Anodes Doubler

This section is dedicated to a brief discussion of the expected performances of the receiver, based on the simultaneous simulations of the 600 GHz two anodes doubler and the 1.2 THz mixer. The improvement associated to a new set of diodes of the 1.2 THz mixer with physical parameters closer of the nominal set used in section 6.6 is also discussed in this section. The input power in the 600 GHz doubler has been analytically defined with a square polynomial matching to reproduce an approximation of the experimental value along the frequency band presented in section 3.2.4 (Fig. 3.19).

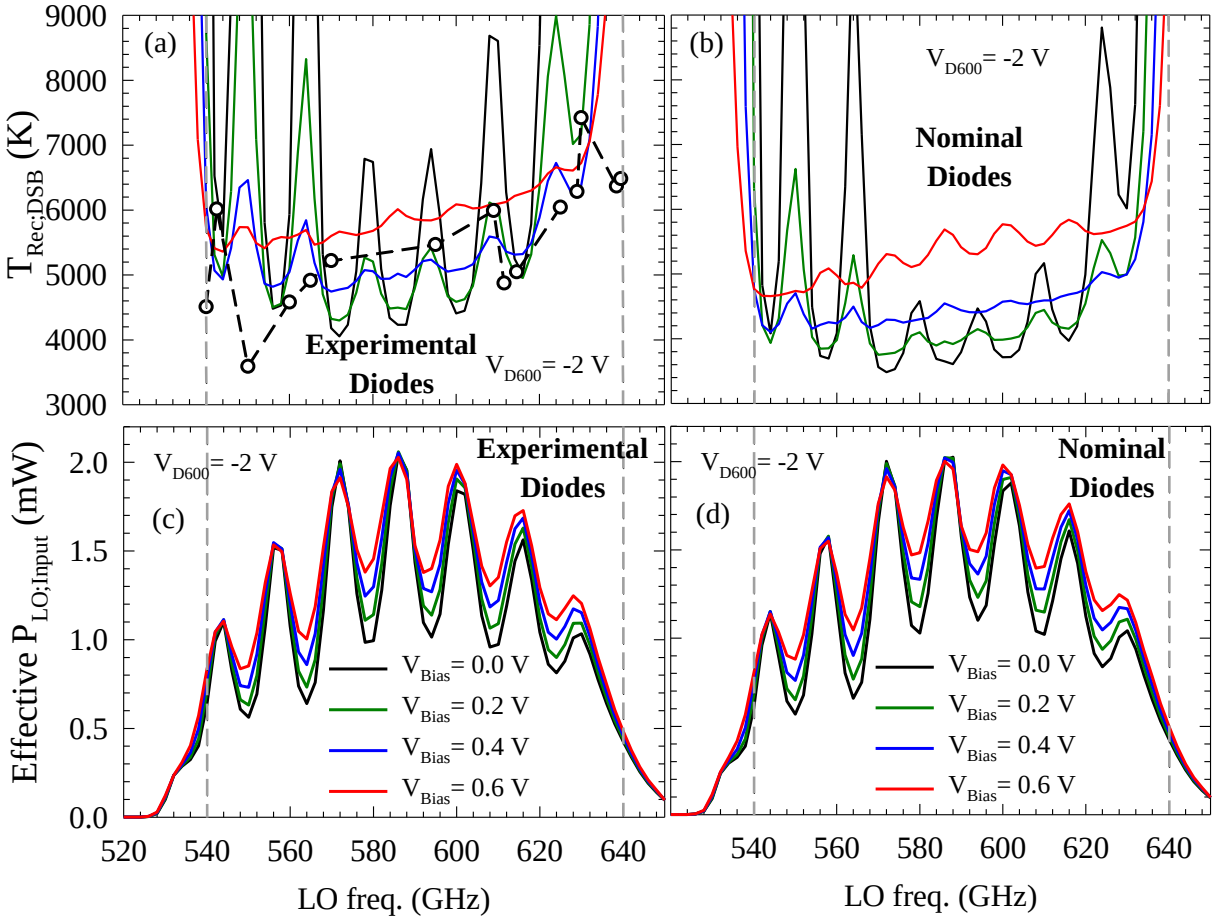

Fig. 6.40. DSB noise temperature obtained with the simultaneous simulations with the set of physical parameters used for the 1.2 THz mixer based on the experimental I-V characteristics (a) and the nominal set of parameters (b). Effective LO input power delivered by the 600 GHz two anodes doubler in simultaneous simulations of the 1.2 THz receiver with the set of parameters based on the experimental I-V characteristics

(c) and the nominal set of parameters (d). The 1.2 THz mixer diodes are bias at different values while the 600 GHz two anodes doubler is at a fixed -2 V bias. The simulations consider room temperature conditions.

The simulated DSB noise temperature of the receiver along the frequency band and the effective LO input power delivered to the 1.2 THz mixer are plotted in Fig. 6.40. The bias of the 600 GHz doubler diode cell is fixed at -2 V in all cases, since it has been found to be the constant value that gets almost the best simulated performances of the receiver along the frequency band in accordance with the variation of the defined LO input power in the 600 GHz doubler. Four different biases of the 1.2 THz mixer diodes from 0 V to 0.6 V have been considered to analyze its influence in the performances of the receiver. The effective LO input power delivered by the 600 GHz two anodes doubler to the 1.2 THz mixer is plotted in Fig. 6.40(c) and 6.40(d) for the experimental set of parameters and the nominal values, respectively. The interaction between both modules due to the generated standing waves modifies the final effective input power delivered by the doubler. The standing waves induce an oscillation of the effective input power around the values obtained in individual simulations of the 600 GHz doubler (section 4.1.4). These oscillations of the available LO power vary from ~1 mW to ~2 mW at cero bias applied, but this minimum value can be increased when biasing the 1.2 THz mixer diode cell. This means that the interaction with the standing waves generated between both modules induces an average increment of available input power when biasing the 1.2 THz mixer diodes. However, this does not mean that when biasing the 1.2 THz mixer diodes it is possible to obtain the best performance of the receiver as it is possible to view in Figs. 6.40(a) and (b) for the experimental set of parameters and the nominal values, respectively. The frequencies where the available input power is very reduced, due to the standing waves between both modules, cannot be minimized even if the available input power increases when the 1.2 THz mixer bias increases. This is because a positive bias of the 1.2 THz mixer diodes induce a higher contribution of the diodes to the noise delivered to the IF port. This results in an optimal DSB noise temperature that oscillates along the band. These oscillations are larger when considering the experimental set of simulation parameters of the PSBDs model than in the nominal case.

The minimum DSB noise temperature performed by the LERMAs simulated ADS-HFSS 1.2 THz receiver is around 4100 K for the experimental set of parameters and it can be reduced around 3500 K when improving the experimental physical parameters of the Schottky diodes to approach nominal values. The minimum DSB noise temperature values without biasing the 1.2 THz mixer diodes can be obtained when pumping with an effective LO input power ~1.8 mW. The optimal 1.2 THz mixer-bias depends on the available effective LO input power. This can be observed at LO frequencies around 580 GHz, 594 GHz and 609 GHz where the available effective input power at cero 1.2 THz mixer-bias is around 1 mW of LO power and the optimal 1.2 THz mixer-bias is in these cases around 0.15-0.2 V. These values of the bias are very low compared with the expected one in accordance with Fig. 6.38. It is because the effective LO input power increases as the 1.2 THz mixer-bias increases at these frequencies. The 1.2 THz mixer bias is found useless at LO frequencies around 570 GHz, 586 GHz, 600 GHz because there is enough LO power even at cero 1.2 THz mixer-bias. However, the mixer-bias is found to be critical if the effective LO input power is lower than 1 mW at cero mixer-bias, in accordance with Fig. 6.38, especially at the edges of the frequency band. The

experimental DSB noise temperature values presented in section 6.5 can be explained in terms of the studied interaction between the 600 GHz two anodes doubler and the 1.2 THz mixer. The additional interaction with the previous 300 GHz doubler has not been accounted for in this work due to the complexity associated with these kinds of ADS-HFSS test bench and the computational time.

We can then conclude that the DSB noise temperature performed by the experimental receiver presented in section 6.5 is associated to a strong oscillation of the available LO input power along the band due to the standing waves generated between both the mixer and the previous multiplication chain. The lower experimental DSB noise temperature compared with the individual simulations of the 1.2 THz mixer are associated with an improvement in the LO coupling efficiency of the 1.2 THz mixer when interacting with the LO chain. It has also been demonstrated that it is not possible in practice to obtain the optimal performance of the 1.2 THz mixer at room temperature over the band using the 600 GHz two anodes doubler because it cannot deliver enough power along the full frequency band. The maximum DSB noise temperature of the receiver when using the 600 GHz two anodes doubler can be reduced at certain frequency points if the experimental bias circuit is improved to efficiently work without introducing additional noise temperature. However, the increment of the LO chain performance when cooling down is able to correctly pump the 1.2 THz mixer in most of the band, as shown in Fig. 6.35. This means that the actual 600 GHz two anodes doubler could be enough to pump the frequency mixer when the receiver works under cryogen conditions (~120 - 150 K), but it is not enough at room temperature.

6.7.2 Simultaneous Simulations with the 600 GHz four Anodes Doubler

An equivalent analysis has been carried out in this section when considering the simultaneous simulations of the 1.2 THz mixer and the 600 GHz four anodes doubler developed in section 4.2. The DSB noise temperature and the effective LO input power results of the simultaneous simulations over the band are plotted in Fig. 6.41. The results obtained with different set of physical parameters of the PSBDs diode model are compared here again. The simulated parameters of the 600 GHz four doubler are in any case the same values used in section 4.2. Two different sets of parameters are used for the 1.2 THz mixer diodes, the nominal set of parameters presented in section 6.4.5 (Fig. 6.41(b) and (d)), and the set of parameters based on the experimental measurements of the PSBDs I-V characteristics defined in section 6.6 (Figs. 6.41 (a) and (c)). The 600 GHz four anodes doubler bias has been fixed at V_{Bias}= -2.4 V in this case, i.e., -1.2 V per anode. The input power used to pump the 600 GHz four anodes doubler is exactly the same used in the previous section but the effective LO input power delivered by the 600 GHz four anodes doubler is higher in this case along the full band. The effective input power oscillates in this case between 1.4 mW and 3.0 mW at cero mixer-bias. The DSB noise temperature performance at cero mixer-bias is therefore improved due to the higher minimum available LO power. This higher effective LO input power together with the improved effective LO coupling efficiency of the 1.2 THz mixer, in simultaneous simulations, leads to a DSB noise temperature that can be optimized in most of the band. The lack of LO power at some frequency points along the band observed in Fig. 6.40 no longer exists when using the 600 GHz four anodes doubler. The DSB noise

temperature cannot be improved in most of the frequency band when biasing the mixer due to the high effective LO input power. However, a negative bias of the diodes is predicted to be useful at some frequency points to slightly reduce the DSB noise temperature of the receiver. Additionally, it is expected that a calibration of the effective LO input power delivered by the 600 GHz four anodes doubler will be required since it can over-pump the 1.2 THz mixer. This over-pumping of the PSBDs cannot be correctly predicted by using the shot and the thermal noise in the STD model. It predicts an optimal effective LO input power higher than 2.4 mW at cero mixer-bias (Fig. 6.38). It was previously mentioned that an additional source of noise in PSBDs in section 6.4.2 appears when strongly pumping the PSBDs. The Hot-electron thermal noise induces a reduction of the optimal effective LO input power as explained in [Crow87] and [Thom03]. This optimal ef
mW in our 1.2 THz mixer.

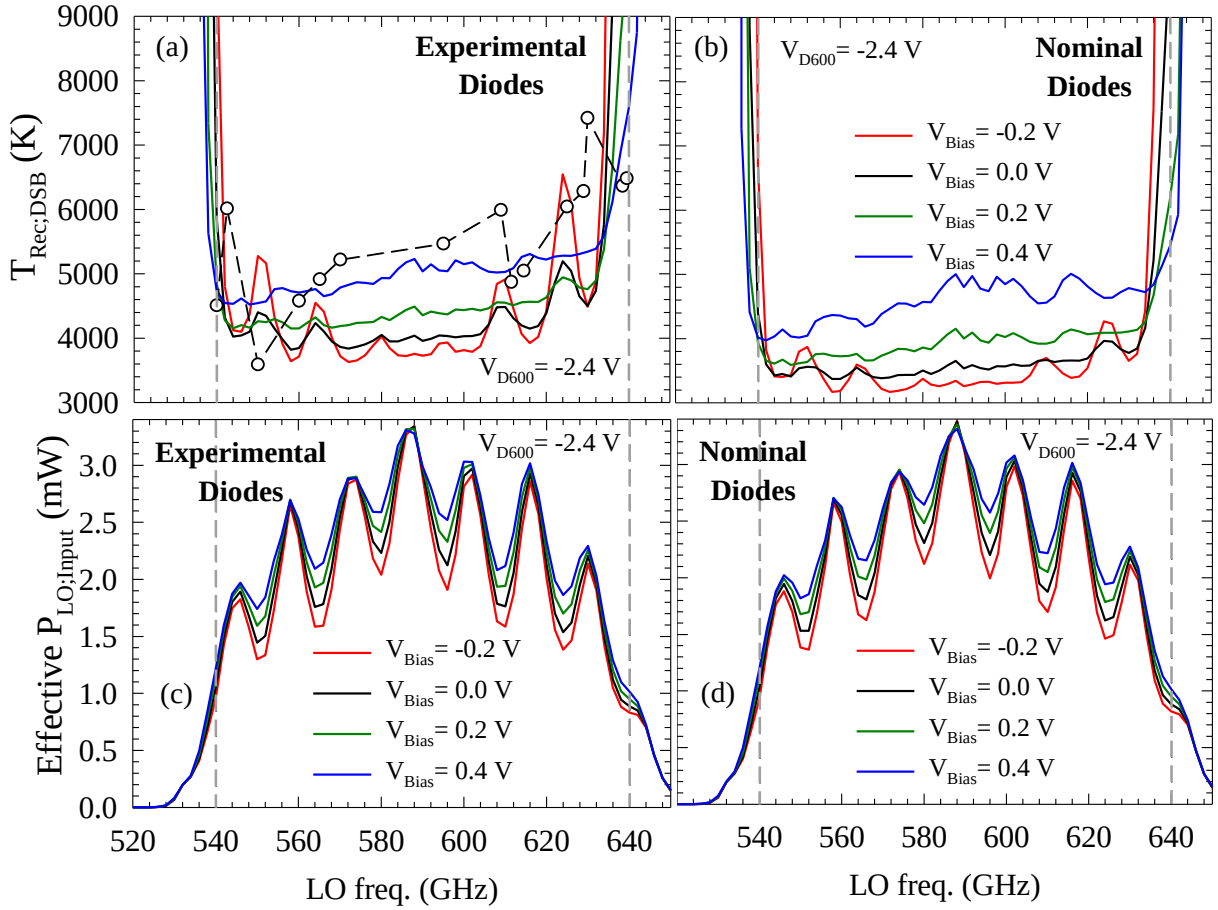

Fig. 6.41. DSB noise temperature obtained with the simultaneous simulations with the set of physical parameters used for the 1.2 THz mixer based on the experimental I-V characteristics (a) and the nominal set of parameters (b). Effective LO input power delivered by the 600 GHz four anodes doubler in simultaneous simulations of the 1.2 THz receiver with the set of parameters based on the experimental I-V characteristics (c) and the nominal set of parameters (d). The 1.2 THz mixer diodes are bias at different values while the 600 GHz four anodes doubler is at a fixed -2.4 V bias. The simulations consider room temperature conditions.

We can conclude that the improved 600 GHz four anodes doubler is expected to correctly pump the 1.2 THz mixer over the frequency band even at room temperature. In fact, a power attenuator would be necessary to optimize the DSB noise temperature of the receiver at the frequency points where there is more than ~1.8 mW of LO input power. A stronger

attenuation of the LO power would be necessary at cryogen temperatures when using the 600 GHz four anodes doubler. The 600 GHz four anodes doubler opens the possibility to redesign a non-biasable 1.2 THz mixer chip where the on-chip capacitor can simply be eliminated and the conversion loss of the receiver reduced. The fabrication of this improved module is therefore critical in the performance of the 1.2 THz mixer at room temperature.

6.7.3 Simultaneous Simulations of the 1.2 THz mixer with Highly Doped PSBDs

An increased epilayer doping of the PSBDs used in the 1.2 THz mixer design is proposed in this section. The impact of a $5{\cdot}10^{17}$ cm^{-3} epilayer doping on the receiver performances when simultaneously simulating the 600 GHz four anodes doubler and the 1.2 THz mixer is discussed. It is straightforward to redefine the PSBDs simulation parameters required for the 1.2 THz mixer when increasing the epilayer doping. The same geometry is assumed and the only variations are therefore associated to the increased doping that reduces the series resistance and the relationship between the built-in voltage and the barrier height. The new set of simulation parameters are based on the nominal values previously proposed, and are given by a saturation current I_{Sat}= $1.56{\cdot}10^{-12}$ A, a built-in voltage V_B= 0.75 V, an ideality factor η= 1.4, a junction capacitance C_{j0}= 0.63 fF and a series resistance R_S= 58.6 Ω. The unbalance series resistance is not accounted for in this analysis since the objective is to determine the expected impact on the global performances of the receiver. The simulation results of the DSB noise temperature of the receiver obtained with simultaneous simulations of the 1.2 THz mixer and the 600 GHz four anodes doubler are plotted in Fig. 6.42. The previous results obtained with the PSBDs with $3{\cdot}10^{17}$ cm^{-3} epilayer doping (dashed lines) are compared with the results obtained with $5{\cdot}10^{17}$ cm^{-3} epilayer doping (solid lines).

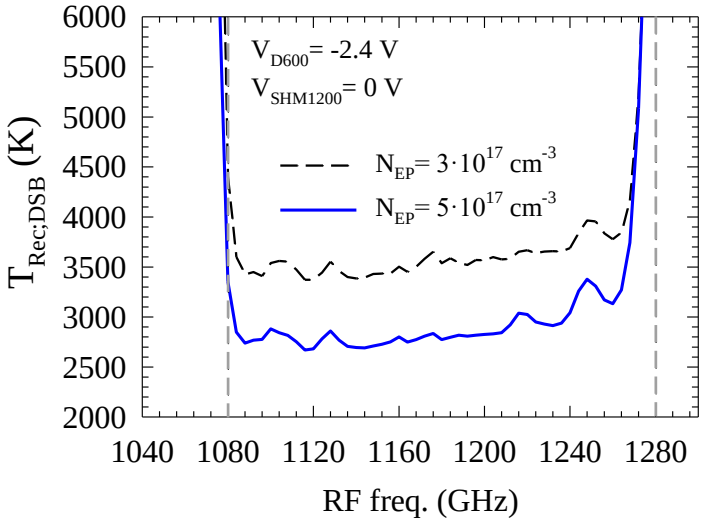

Fig. 6.42. DSB noise temperature obtained with the simultaneous simulations of the 600 GHz four anodes doubler and the 1.2 THz mixer when doping the PSBDs epilayer at $3{\cdot}10^{17}$ cm^{-3} (black dashed line) and $5{\cdot}10^{17}$ cm^{-3} (blue solid line). Cero mixer-bias is considered while the 600 GHz four anodes doubler bias is fixed -2.4 V. The simulations consider room temperature conditions.

The increment of the epilayer doping in the 1.2 THz mixer PSBDs has a significant impact on the DSB noise temperature performed by the receiver. It is reduced up to 800 K in most of the band compared with the previous results and non-appreciable decoupling at higher

frequencies is predicted by these simulations despite increasing the capacitance of the diodes. The improvement of the DSB noise temperature can be associated to the reduced series resistance. This comparison allows us to determine the impact of an increased doping on the 1.2 THz receiver performance but it is difficult to accurately predict the quantitative experimental improvement. No saturation phenomena are accounted for in the considered PSBD model and its influence is different between two different epilayer doping levels. This means that the results compared in Fig. 6.42 do not take into account the different impacts of saturation phenomena associated to each epilayer doping. Additionally, the hot-electron thermal noise is not accounted for in these simulations and the optimal effective LO input power can also be slightly increased when increasing the doping level since the capacitance is increased and the series resistance is reduced (see section 6.4.2).

6.8 Updated Experimental Status of the 1.2 THz receiver

The experimental results presented in this section have been obtained several months after the results discussed in previous sections of this dissertation. This section presents the improved performance obtained with the developed 1.2 THz receiver after a new fabrication run of the MMICs of the LERMA's 1.2 THz mixer. Additional modifications of the test bench have also been included to address the malfunctioning of the mixer bias. It was found that the LNA used at cryogenic temperatures allowed to correctly bias the 1.2 THz mixer while the LNA used at room temperature didn't allow biasing the same mixer. This fact indicates that the LNA used at room temperature doesn't have an integrated input capacitor while the LNA used at cryogenic temperatures has it. This has allowed measuring the new set of MMICs of the 1.2 THz mixer using the bias circuit at cryogenic temperatures. However, the main improvements are associated to the new MMICs of the mixer. First, the fabrication process was thoroughly reviewed by Dr. L. Gatilova at LPN looking for the maximum performance of the PSBDs integrated in the chips. Second, a new wafer with an increased epitaxial doping up to $5{\cdot}10^{17}cm^{-3}$ was fabricated by Dr. A. Cavanna at LPN. The Schottky anodes were reduced to reproduce the junction capacitance of the previous $3{\cdot}10^{17}cm^{-3}$ based in the improved performance predicted by this author in section 6.7.3 using HFSS-ADS simulations. A diagram of the mechanical montage of the receiver used for cryogenic measurements is indicated in Fig. 6.43. The montage is very similar to the test-bench presented in Fig. 6.34(a). The LERMAs' receiver is cooled down while the RPGs' source remains at higher temperatures. The E-band booster amplifier has been removed to correctly place the source and the receiver inside the cryostat. The RPG AFM-90 tripler has been self-biased using a 2.7 kΩ resistor to have more available Keithley power supplies. The mixer-bias has also been thoroughly analyzed to reduce any additional voltage noise introduced by the power supply used at LERMA. A voltage divider has been chosen to bias the 1.2 THz mixer. The proposed voltage divider not only allows biasing the diodes with a fraction of the voltage provided by the power supply but also the voltage noise is reduced in this fraction.

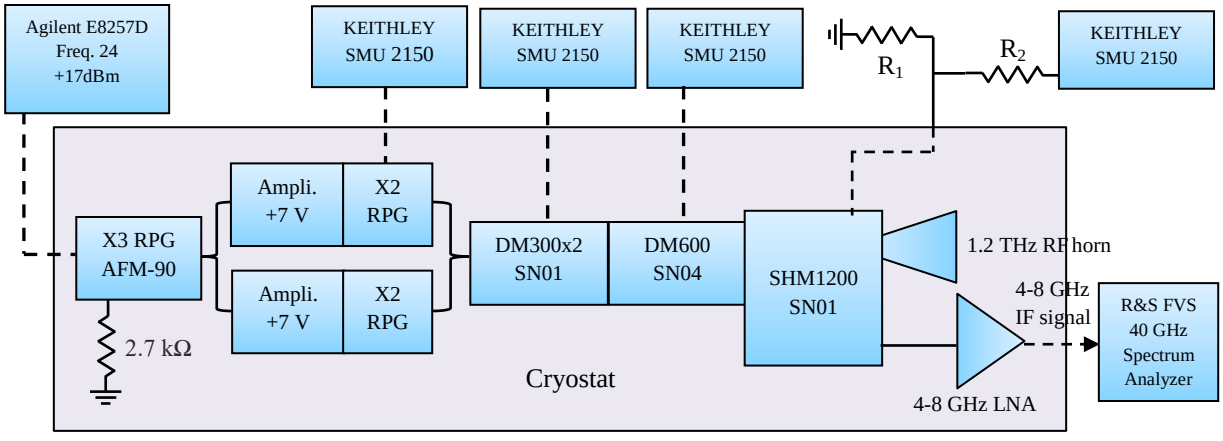

Fig. 6.43. Diagram of the experimental test bench used for the cryogenic temperature measurements of the 1.2 THz receiver at LERMA.

6.8.1 Local Oscillator Chain

The local oscillator chain has been reviewed and experimentally studied to efficiently provide the maximum LO power for the cryogenic characterization of the receiver. It has been experimentally observed at LERMA that the LO chain is able to provide more power than required at certain frequency points during cryogenic measurements even if the E-band booster amplifier is not included. This means that a tunable attenuator would be required for correctly operating the LO chain at cryogenic temperatures including this amplifier. However, this option has not been possible to be implemented at LERMA due to the reduced space inside the cryostat. The E-band booster amplifier has not been included in these measurements like in the previous results presented in section 6.5. This has required special attention to be paid to the first stage of the LO source to provide the maximum available power to the E-band amplifiers. The initial signal required to pump the RGP AFM-90 tripler between 22.5 GHz to 26.67 GHz is generated by the Agilent E8257D synthesizer. A one meter K-type cable has been required to lead the signal from the synthesizer to the RPG AFM-90 tripler inside the cryostat. It was determined that up to 6 dB losses are introduced by this K-type cable which has required to use the synthesizer at maximum power (23 dBm). The RPG AFM-90 tripler is homogenously pumped with 17-18 dBm between 22.5 GHz to 26.67 GHz. This tripler has been thoroughly analyzed to efficiently provide the power along the frequency band. The self-bias option was considered and several resistors from 1-3 kΩ were used to analyze the provided power at room temperature. The value 2.7 kΩ was finally selected because it is the best self-bias point to keep the higher frequencies of the band, especially at 78.5 GHz required for the methane line. The experimental results of RPGs tripler are not included in this dissertation since it is not LERMAs property. The provided power by this tripler is amplified and doubled by RPG doublers to reach the frequency band 135 – 160 GHz. This source is used to pump the LERMA's LO chain consisting of the 300 GHz power-combined doubler and 600 GHz doubler. The output power provided by four different modules of the 600 GHz doubler are plotted in Fig. 6.44.

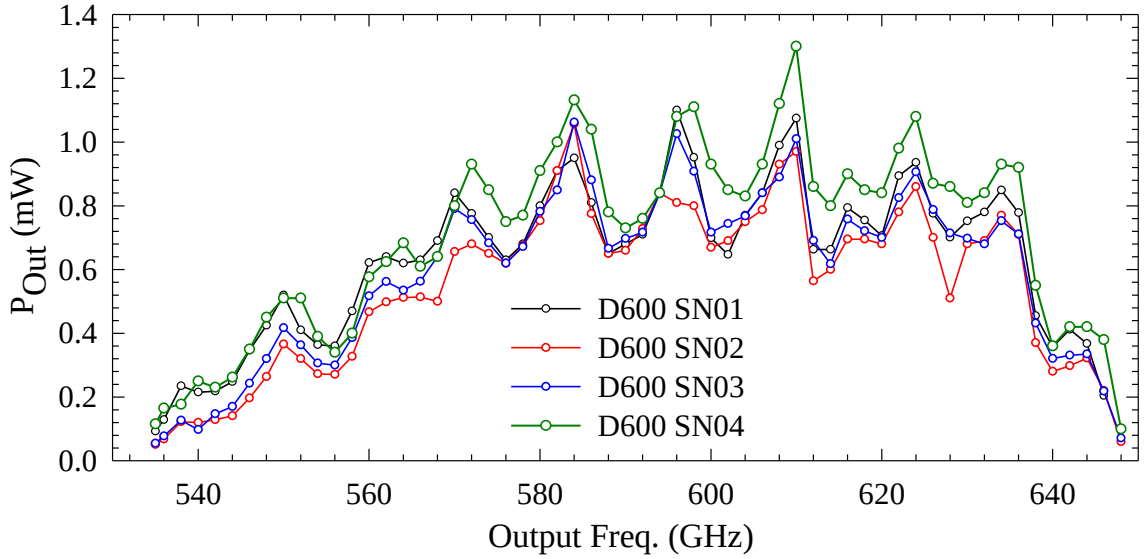

Fig. 6.44. Output power delivered by the 600 GHz LO chain at room temperature without E-band booster amplifier.

The results presented in Fig. 6.44 have been automatically measured using the LabVIEW software. It has been previously confirmed that the optimal bias does not significantly change between different modules. This is the reason for the optimal bias values previously found at each frequency point for the 300 GHz and 600 GHz doublers are used now for each different block. It is possible to observe in Fig. 6.44 a good reliability of the different modules developed by LERMA. The differences observed between each module are mainly associated to the different mechanical blocks and the chips assembly. However, the SN04 module has shown a better performance along the frequency band. This slightly additional LO power provided by the 600 GHz SN04 module is the reason this module has been selected in the receiver characterization at cryogenic temperatures. The expected LO power provided by the LO chain at cryogenic temperatures is higher than the values presented in Fig. 6.44. However, these data were not available yet to be discussed in this dissertation.

6.8.2 I-V Characteristics of the New Set of PSBDs 1.2 THz chips

The new set of MMIC chips of the 1.2 THz mixer has been fabricated at LPN. The epilayer doping has been increased up to $5 \cdot 10^{17}$ cm^{-3} and the anode size reduce at ~0.15 μm^2 to reproduce the junction capacitance of the $3 \cdot 10^{17}$ cm^{-3} version previously developed. This new set of MMIC chips has presented a correct performance of the PSBDs I-V characteristics. The I-V characteristics of the integrated PSBDs in the mixer chip used for the updated cryogenic measurements are plotted in Fig. 6.45.

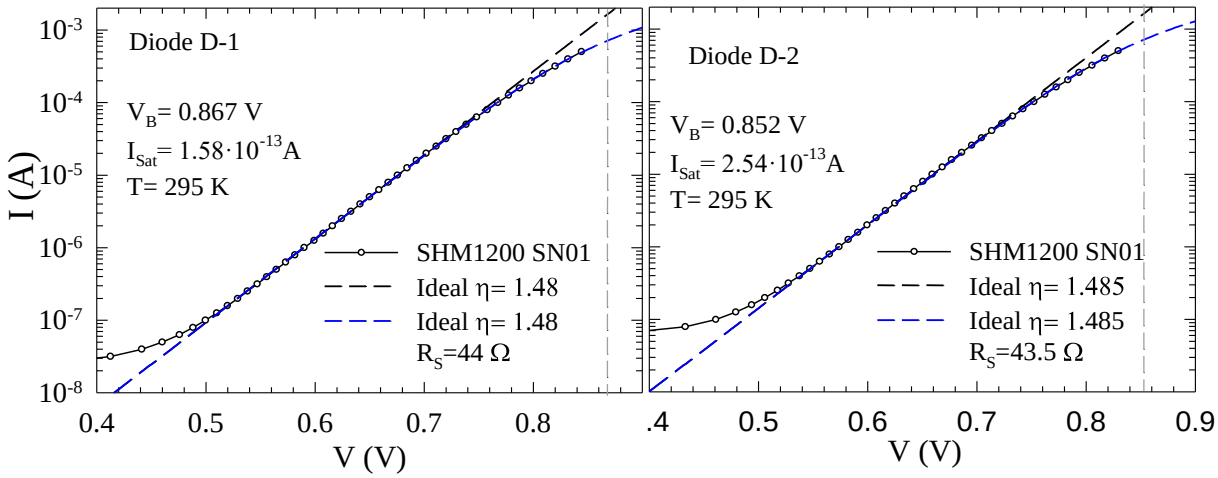

Fig. 6.45. I-V characteristics of the diodes L6C4-A in the 1200 GHz mixer chip mounted in the SN01 block in logarithmic representation. The physical parameters of the diodes are calculated by matching the experimental results (black dots) with the analytical model (dashed blue line). Anode surface 0.145 μm^2.

It is possible to observe a significant improvement of the exponential behavior of the I-V characteristic compared to the previous fabrication shown in section 6.5.1. The expected series resistance for a doping $5 \cdot 10^{17}$ cm^{-3} and a reasonable deviation between the series resistance featured by each diode of the antiparallel configuration have been achieved by LPN. The series resistance is even smaller than expected in Fig. 6.42. The improved quality of the exponential behavior of the I-V and the reduced series resistance in the PSBDs should improve the performance of the chip for the IF generation.

6.8.3 Updated Results of the 1.2 THz receiver at 150 K

The new MMIC 1.2 THz chips have been used in the frequency mixer of the 1.2 THz receiver described in Fig. 6.43. The mixer bias is available in these measurements since the LNA used at cryogenic temperatures has an integrated capacitor that allows the diodes to be correctly biased in series configuration. A voltage divider circuit has been defined as indicated in Fig. 6.43 with R_2= 3.33 kΩ and R_1= 333 Ω. This defines a factor ten between the voltage defined by the external power supply and the bias voltage of the diodes. This bias configuration also reduced by the same factor the voltage noise potentially introduced by the power supply. The external power supply range required to bias the diodes has been experimentally found around 9-10 V in most of the point at cryogenic temperature. A bias of 0.55 V of the diodes in series was experimental observed testing the voltage divider in the mixer when applying an external power supply of 10 V at room temperature. The exact values couldn't be experimentally obtained at cryogenic temperature since it is required to know the experimental I-V characteristic of the diodes to correctly estimate the solution of the voltage divider circuit. However, it can be expected a higher bias through the diodes at cryogenic temperatures because the slope of the I-V characteristic increases as the temperature decreases. The experimental measurements of the noise temperature of the receiver have been obtained as previously explained in section 6.5.3 to determine the Y-factor. The experimental results are presented in Fig. 6.46. The raw measurements of the DSB noise temperature are given by the dotted black line. These measurements demonstrate a significant improvement in the performance of the receiver due to the improved performance of the 1.2 THz mixer and the bias capabilities. However, the real DSB noise temperature of the receiver has to be estimated in accordance with the test-bench used for these measurements. The red dotted line represents the corrected DSB noise temperature accounting for the air transmission loses and the interaction with the cryostat window.

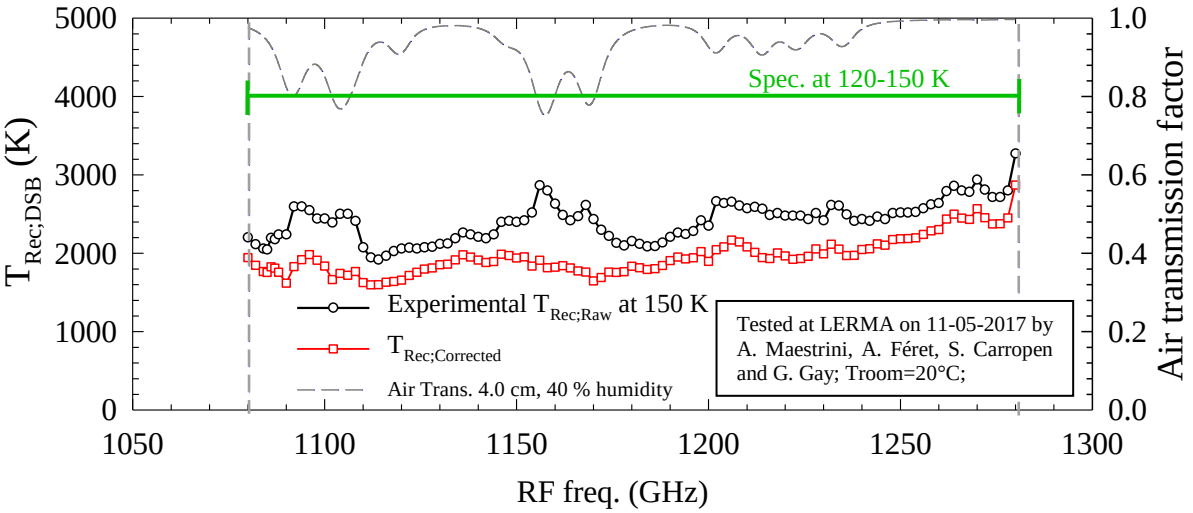

Fig. 6.46. Experimental DSB noise temperature (black line) measured with a power-meter along the RF frequency band at cryogen temperature (~150 K) with the test bench indicated in Fig. 6.43. The corrected DSB noise temperature (red line) accounts for the air transmission coefficient (grey dashed line) of the USB and LSB frequencies in the 4-8 GHz IF frequency range. A 7% flat loss is introduced by the cryostat window.

The air transmission when considering a 4 cm path between the cold source and 40 % humidity in the laboratory has been calculated with the *am* Atmospheric model [Pain17] and plotted (grey line) in Fig. 6.46. The specifications of the project at 120-150 K cryogenic temperature are indicated by the green line around 4000 K DSV noise temperature of the receiver. The cryostat window has been reviewed and improved with a new quartz 3 mm window with ε=4.6 and $6 \cdot 10^{-5}$ lost tangent. This window contains a 5 % loss 250 μm thick Zitex antireflection coating. A flat 7 % transmission loss through this window has been experimentally measured along the frequency band and included in the corrections. The transmission losses though the cryostat window have been significantly reduced in these measurements compared to the results presented in section 6.5.4. This allows a smaller correction factor of the experimental raw measurements. These corrections have finally led from raw DSB noise temperature measurements between 2000 - 2800 K along the band to corrected values between 1800-2400 K at 150 K cryogenic temperature. The improved performance of the 1.2 THz MMIC chips together with the available bias of the mixer have significantly reduced the DSB noise temperature of this receiver compared to the previous version presented in Fig. 6.35. These improvements have also allowed the DSB noise temperature measurement every 1 GHz to demonstrate the continuity of the band performed by this receiver. The Methane line at 1256 GHz is also correctly resolved by this receiver preforming a DSB noise temperature value (2242 K) almost half of the proposed value (4000 K) in the specification of the project. This improved performance has a significant impact in the integration time required by the receiver to obtain science data. The integration time equation in radioastronomi is given by:

$$\tau \propto \frac{1}{\Delta\nu}\left(\frac{T_{Sys}}{\Delta T}\right)^2 . \qquad (6.25)$$

This means that the integration time τ required resolving the methane line with a specific brightness temperature ΔT using a bandwidth Δυ in a sample is almost four times smaller than the expected in the project specifications since the integration time has a square dependence on the system noise temperature T_{Sys}.

Regarding the LO chain, the montage used for this measurements is not the defined fly version of the receiver. The final version uses a USO to pump a Ku-band synthesizer able to open the frequency band. This source is then used to pump the RPG source including the E-booster amplifier in Fig. 6.43. This leads to a higher available LO power at 600 GHz that would require a tunable attenuator at cryogenic temperatures. Additionally, the implementation of the 600 GHz four-anodes doubler proposed by this author in Chapter 4 is expected to increase the efficiency of the LO chain. These improvements could potentially eliminate the bias requirements of the 1.2 THz mixer. This would reduce the power requirements of the receiver.

6.9 Conclusions

The PSBDs properties required to optimize the design of a 1.2 THz mixer have been discussed in section 6.1. The experimental minimum Schottky anode size that can be fabricated has been determined as the main constraint of this design. The smallest Schottky anode size was initially fixed at ~0.2 μm^2 by LPN. A $3 \cdot 10^{17}$ cm^{-3} epilayer doping has been demonstrated to be the most suitable option for the optimization of the MMIC mixer chip in accordance with this limitation in the anode size fabrication. However, the improved conversion efficiency of the RF into the IF signal has been demonstrated if the anode size is reduced.

Two different designs of the 1.2 THz mixer chip were developed and described in section 6.2. The main design considerations for each case have been discussed within this section and it has been concluded that the LERMAs "Out-channel" design of the 1.2 THz mixer is the most suitable option to be developed in practice because the bandwidth can be extended more than in the "In-channel" version. A $3 \cdot 10^{17}$ cm^{-3} epilayer doping of the PSBDs was considered for optimizing the MMIC chip. The design of the mechanical block to define the IF and the DC circuits has been presented in section 6.3.

The most important concepts when analyzing the performances of a frequency mixer and receiver are detailed in section 6.4. The conversion loss is discussed in section 6.4.1 and applied in section 6.4.4 for the ADS-HFSS analysis of the designed 1.2 THz mixer. The definition of the noise temperature of the receiver is detailed in section 6.4.3 and it is applied in section 6.4.5 for the ADS-HFSS analysis of the designed 1.2 THz mixer. The impact of a simulated RLC circuit in the PSBD model of the series impedance is finally discussed in section 6.4.6.

The experimental results obtained with the first functional LERMA's 1.2 THz receiver which consists of a 1.2 THz mixer, a 600 GHz two anodes doubler and a 300 GHz power-combined doubler are presented in section 6.5. The I-V characteristics analysis of an experimental representative 1.2 THz mixer chip is carried out in section 6.5.1. The experimental physical parameters required to reproduce the obtained I-V characteristics notably deviate from the expected nominal values. Different series resistances have also been featured for each PSBD of the experimental 1.2 THz mixer chips. The bias circuit of the first 1.2 THz mixer modules was not used due to a lack of integrated capacitor in the LNA used at room temperature. The experimental DSB noise temperature measurements at room temperature of a 1.2 THz receiver, when pumping with the RPG source, are presented in section 6.5.3. DSB noise temperature between 5000 - 6000 K was performed by the presented receiver at room temperature. The experimental DSB noise temperature measurements at cryogenic temperature of the 1.2 THz receiver, when pumping with the RPG DM driver chain, are presented in section 6.5.4. DSB noise temperature between 3000 – 4000 K was found at cryogenic temperatures of the presented receiver.

A comparison between the experimental results and the individual ADS-HFSS simulations of the designed LERMA 1.2 THz mixer chip is carried out in section 6.6. Equivalent comparison has been carried out in section 6.7 accounting for ADS-HFSS simulation where the 600 GHz doubler is included together with the 1.2 THz mixer. This analysis has demonstrated that the behavior of the experimental 1.2 THz receiver cannot be explained in terms of individual simulation of the frequency mixer. The overall performance of the receiver has been demonstrated to be substantially modified when simulating the LO chain together with the frequency mixer. The LO coupling efficiency of the 1.2 THz mixer has been demonstrated to be improved due to the interaction with the LO signal generated by the 600 GHz doubler. This results in a higher performance of the receiver DSB noise temperature than expected in individual simulations of the mixer when pumping with the same effective LO

input power. However, the interaction between both modules induces a strong oscillation of the available effective LO input power used to pump the 1.2 THz mixer along the frequency band. Regarding these oscillations, it has been demonstrated in section 6.7.1 that the effective LO power oscillations along the band can induce a lack of LO power at some frequencies when using the 600 GHz two anodes doubler at room temperature. It can be mitigated by biasing the 1.2 THz mixer diodes but the maximum performance of the mixer cannot be obtained. However, the 600 GHz two anodes doubler can deliver enough LO power at cryogenic temperatures as demonstrated in section 6.5.4. Alternatively, the lack of effective LO input power can be substantially reduced along the band at room temperature when using the redesign 600 GHz four anodes doubler. No mixer-bias is expected to be required in this case and it opens the possibility of improving the mixer performance since the on-chip capacitor can be removed and the conversion loss of the mixer improved. The increment of the epilayer doping of the PSBDs is expected to improve the receiver performance, as discussed in section 6.7.3.

A second generation of the 1.2 THz mixer has been characterize in section 6.8. A new set of 1.2 THz MMIC chips at $5 \cdot 10^{17}$ cm^{-3} epilayer doping have been fabricated. The I-V characteristics of these PSBDs have been discussed in section 6.8.2. The PSBDs characteristics have performed a significant improvement compared with the first generation. The mixer bias was available in the cryogenic measurements of these new mixers since the LNA used at low temperatures features an integrated input capacitor. A final DSB noise temperature between 1800 – 2400 K has been demonstrated by this receiver at LERMA. Further improvements in the LO chain are expected in the future, including the 600 GHz four-anode doubler proposed by this author. The implementation of this doubler together with the E-band booster amplifier and a bias-controlled attenuator can potentially eliminate the bias requirements of the mixer at cryogenic temperatures.

7 Conclusions and Perspectives

The initial LERMA assignment as part of the SWI consortium at the end of 2013 was the development of a 300 GHz doubler and the industrial delivery of the ultra-stable local oscillator and the Ku-band synthesizer of the SWI instrument. However, LERMA has additionally developed a 600 GHz doubler and 600 GHz and 1.2 THz mixers during this project. Moreover, LERMA successfully demonstrated the 1.2 THz channel in May 2016 and received approval for the SWI 1.2 THz channel delivery. The chronological development of these achievements has been embodied in this dissertation. Initially, the experience obtained by LERMA-LPN collaboration in the design and fabrication of experimental Schottky-based THz modules, together with the theoretical experience provided by the Department of Electronic at the University of Salamanca was the starting point for this work. The inclusion of this author in LERMA's Schottky group was accompanied by the introduction of a 2D-MC simulator in collaboration with the University of Salamanca, Spain. In the framework of LERMA's and University of Salamanca collaboration, the physical model of the Schottky diodes was studied in accordance with the experimental PSBD structures developed by LPN. First, the analytical equations of the PSBDs' capacitance model, required by the HB-ADS simulator, were extended as a result of the theoretical analysis carried out by this author based on 2D-MC simulations. Part of this MC study was published during this dissertation. Second, the analytical current and capacitance equations were consistently implemented in the ADS simulator aiming for an extended model able to more accurately predict the diodes' response in THz application. Finally, this model has successfully demonstrated its increased prediction capabilities in varactor mode applications.

This model was first validated when studying the developed 300 GHz doubler presented in Chapter 3. Dedicated experiments demonstrated the improvement of the developed PSBD model to accurately predict the optimal bias of the doubler. Second, the developed PSBD model proved to be critical in the prediction of the diodes response and therefore, the conversion efficiency performed by these PSBDs. The analysis of the previously developed design of a 600 GHz two-anodes doubler was presented in chapter 4 using the extended capacitance model. The additional capacitance featured by the PSBD during one period of the input signal due to the edge effect is accounted for by this model and it has proven to negatively impact the conversion efficiency of the doubler. The substrate effect has also been implemented in the model. However, the substrate effect can only appear when substantially reducing the epilayer thickness, which is not the case in the developed LERMAs doublers. Nevertheless, the first version of the experimental 600 GHz LO power source presented in section 4.1 is able to deliver more than 1 mW LO power in most of the frequency band at room temperature with 6-8 % conversion efficiency. However, it has been shown by this author that the presence of standing waves between the previous multiplication stages and the 600 GHz doubler are responsible for a reduced power under 1 mW at certain frequencies. Finally, the preliminary results of the developed 600 GHz LO encouraged this author to propose an alternative design of a 600 GHz four-anodes doubler able to handle higher power with higher conversion efficiency. This design is expected to ensure more than 1 mW LO power in the full band using RPGs source. The knowledge obtained concerning varactor doublers during this work has allowed this author to define a new set of diodes devoted to a redesigned high efficiency four-anodes doubler at 600 GHz. The physical properties and geometry of the epilayer were modified and the optimization of the MMIC chip was carried out considering the extended PSBD model. The resulting 600 GHz four-anodes doubler has been compared in section 4.2 with the previously developed 600 GHz two-anodes doubler in the same simulation conditions and an efficiency twice as large is expected to be performed by this design.

Regarding the usefulness of the developed model in the design of Schottky mixers, it has been concluded in this dissertation that a further extension of the PSBD model accounting for saturation phenomena is required when aiming for an accurate prediction of the diodes' response. Additionally, an extended noise model of the mixer consistently integrated with the HB simulator is required as demonstrated by Dr. D. Pardo. However, it has been discussed in Chapter 5 and 6 that an accurate prediction of the junction capacitance accounting for the edge effect as well as a consistent relationship between the simulated current and capacitance characteristics can significantly improve the prediction capabilities. This is especially true when defining the frequency range of the application and the epilayer properties of PSBDs. The implementation of the substrate effect in frequency mixers has not been found to substantially improve the prediction capabilities of the model since it does not significantly modify the PSBD response compared to the edge effect. This is because the diode response is mainly determined by the non-linearity of the I-V characteristic around flat band while the substrate effect only modifies the average capacitance which is mainly defined by the junction and the edge effect capacitance. The development of an experimental 600 GHz mixer based in Dr. J. Treuttel's design has been critical for this work to study frequency mixers performances using the developed PSBD model. The additional capacitance due to edge effects significantly modifies the average impedance of these diodes due to the small anode area (~0.5 μm^2) featured in this application. However, a slight reduction of the conversion efficiency of the RF into the IF signal by the PSBDs has been observed when accounting for the substrate effect. The importance of the PSBDs' properties has been systematically studied in Chapter 5 based on the developed model in this dissertation. Finally, three main statements have been proposed by this author in section 5.4 defining the PSBDs' properties and geometry for frequency mixers.

These three statements have been employed in the definition of PSBDs for the 1.2 THz mixer and they were implemented in the design of two different MMCI chips presented in Chapter 6. The design of the Out-channel version was developed in a collaboration between Dr. A. Maestrini and this author while the In-channel version was fully developed by this author. The development of two different versions was encouraged for two main reasons. First, the accomplishment of a 1.2 THz mixer version based in the classical "In-channel" configuration of the MMIC chip previously used in the 600 GHz mixer and also proposed in the framework of this project contract. Second, the demonstration of the advantages provided by the Out-channel version featuring a novel configuration of the MMIC chip. Both versions of the 1.2 THz mixer designs were developed during this work and compared by this author in the same simulation conditions. It has been demonstrated by this author the improved bandwidth provided by the Out-channel version of the 1.2 THz mixer compared to the In-channel version. This allowed to finally select the Out-channel version for the experimental development of the application. The predicted performance of these designs is a noise temperature between 3000 K and 3500 K at room temperature. The first experimental prototype of the 1.2 THz mixer based in the Out-channel chip version was affected by several fabrication defects that led to a reduce performance. First, an abnormally high average series resistance was featured by most of PSBDs together with a significant deviation between the series resistance of each diode in the same chip. Second, a defected bias circuit did not allow mitigating the negative impact of the low available LO power to pump the 1.2 THz mixer. Nevertheless, the preliminary results of the first functional receiver obtained at LERMA covered the full required frequency band between 1080-1280 GHz, presenting around 5000 K at room temperature and less than 4000 K noise temperature at 160 K cryogenic temperature without any mixer-bias. These experimental results have demonstrated the feasibility of the 1.2 THz channel for SWI in May 2016 and have been presented in Chapter 6 of this dissertation. The achievements obtained by LERMA in the development of this prototype

finally gained the CNES financial support of LERMAs contribution in summer 2016 for the 1.2 THz channel delivery. A third trial of the 1.2 THz mixer was accepted for this assignment. The experimental characteristics featured by the PSBDs of this first functional 1.2 THz receiver together with the dysfunctional bias circuit were implemented in the ADS-HFSS simulator and thoroughly studied by this author to explain the obtained experimental results and determine any source of improvement for the next fabrication setup.

A novel study of the interaction between the LO chain and the frequency mixer has been carried out in section 6.7 by this author and it has been concluded that the simultaneous simulation of the 600 GHz doubler and the 1.2 THz mixer induces a higher LO coupling efficiency with the mixer. This leads to a lower requirement of the bias circuit since the mixer is able to couple the LO power more efficiently than predicted by individual simulations of the mixer. However, the interaction between the 600 GHz doubler and the 1.2 THz mixer produces significant standing waves that induce an unexpected lack of LO power at certain frequencies along the frequency band. It has been demonstrated by this author that the negative impact of this lack of LO power at certain frequencies due to the standing waves cannot be avoided at room temperature even if the bias circuit was functional. This is because the provided power by the LO chain using the 600 GHz two-anodes doubler is within the limit of the required power at room temperature. However, the developed LO source is able to correctly pump the mixer at cryogenic temperature even if no bias is available due to the improved performances of the multipliers at low temperatures. A redesign of the 600 GHz doubler featuring four anodes has been developed by this author and proposed in Chapter 4 to offer an alternative to improve the LO chain performances. This new design is expected to provide higher conversion efficiency than the developed 600 GHz two-anodes doubler and sufficiently pump the 1.2 THz mixer even at room temperature. The potential development of this new version of the 600 GHz doubler allows the possibility of a simplified version of the 1.2 THz receiver without on-chip capacitor, i.e., without bias circuit. An intrinsic improvement of the receiver performances can be obtained if the bias circuit is removed. This is because any voltage noise introduced by the bias source is eliminated and the losses associated with the on-chip capacitor are avoided. Finally, an increment of the PSBDs' doping level up to $5 \cdot 10^{17}$ cm^{-3} has been proposed in section 6.7.3 by this author since an improved performance of the receiver has been predicted with this modification.

The implementation of all the gathered knowledge in the fabrication of the 1.2 THz MMICs and assembly resulted in a new fabricated set of chips in May 2017. The increment of the epilayer doping up to $5 \cdot 10^{17}$ cm^{-3}, with the corresponding anode size reduction (~0.15 μm^2), has been achieved by LPN in this fabrication run leading to a reduced series resistance compared to the $3 \cdot 10^{17}$ cm^{-3} doping version while maintaining similar junction capacitance. Additionally, the new set of MMICs chips present an adequate value of series resistance in the PSBDs without significant deviations between the anti-parallel diodes placed on the chip. Additionally, the bias circuit was functional for cryogenic measurements of the DSB noise temperature of the receiver. All these improvements together have significantly improved the performance of the LERMAs receiver at 1.2 THz performing less than 2000 K DSB noise temperature at 150 K for part of the frequency band and less than 2500 K in the required band between 1080-1280 GHz. The scientific interest of this channel in the methane line at 1256 GHz has been addressed with this receiver featuring a noise temperature almost half of the required value at 150 K. This increment of twice in the receiver sensitivity compared to the initial specifications of the project reduces in four times the integration time required to obtain the same spectral information quality of the RF signal. This leads to a higher quality and larger amount of science data that can be gathered by the developed 1.2 THz receiver for SWI.

Additional improvements are expected in the future. First, the fabrication of the engineering model is ready once the different components of the receiver are demonstrated. This consists in the technical definition of all components power requirements and the optimization of the fly version assembly of the 1.2 THz channel. The fly version includes the USO to generate the initial frequency signal that is used by a Ku-band synthesizer to provide the required frequency band for SWI. The RPG source includes the E-band booster amplifier removed at LERMA for cryogenic measurement and a voltage controlled attenuator is proposed to control the LO power provided to the 1.2 THz mixer. Additionally, all power supplies and control systems of the receiver have to be consistently integrated with the other elements of the SWI instrument. This is necessary to obtain the Technology Readiness Level (TRL) 5 required by the Space program for the SWI instrument. This includes the experimental testing of the SWI instrument in a simulated environment where all technological components are integrated and assembly in a realistic way. All these technical optimizations of the engineering model of the channel should lead to additional LO power compared to the power availability for the cryogenic measurements carried out at LERMA and presented in section 6.8. Second, the fabrication of the 600 GHz four-anodes doubler proposed by this author has been scheduled at LPN. This version of the 600 GHz doubler is expected to perform higher conversion efficiency, leading to higher available LO power to pump the 1.2 THz mixer. This improvement of the LO chain of the receiver could reduce or even eliminate the bias requirements of the mixer, which could simplify the engineering model of the receiver.

Finally, the knowledge accumulated during development of a 1.2 THz channel for SWI lays the basis for future submillimeter wave instruments at higher frequencies. For instance, the 600 GHz LO chain of the 1.2 THz channel of SWI could be redefined at 900 GHz to provide LO power for a 1.9 THz receiver. This channel is scientifically relevant at the present time to study the atomic fine-structure of the ionize Nitrogen and Carbon. This channel has been encouraged by the German REceiver for Astronomy at Terahertz Frequencies (GREAT) instrument for SOFIA observatory [SOFIA2017].

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Appendix

Paper:

Monte Carlo Study of 2-D Capacitance Fringing Effects in GaAs Planar Schottky Diodes,

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Monte Carlo Study of Two-Dimensional Capacitance Fringing Effects in GaAs Planar Schottky Diodes

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***Abstract*— Nanometer scale planar Schottky barrier diodes with realistic geometries have been studied by means of a two-dimensional ensemble Monte Carlo simulator. The topology of the devices studied in this work is based in real planar GaAs Schottky barrier diodes used in THz applications, such as passive frequency mixing and multiplication, in which accurate models for the diode capacitance are required. The intrinsic capacitance of such small devices, which due to edge effects strongly deviates from the ideal value, has been calculated. In good agreement with the classical models, we have found that the edge capacitance is independent of the properties of the semiconductor beneath the contact and, as novel result, that the presence of surface charges at the semiconductor dielectric interface can reduce it almost 15%. We have finally provided a compact model for the total capacitance of diodes with arbitrary shape that could be easily implemented in design automation software such as ADS.**

***Index Terms*— GaAs Planar Schottky diodes, Monte Carlo (MC) simulation, Edge Effect, Capacitance (C-V), JUICE-SWI.**

I. INTRODUCTION

Vast advancements have been done in the development of planar Schottky barrier diodes (PSBDs) for THz local oscillators and heterodyne receivers since this technology was introduced in the 90's, thus finally replacing the whisker-contacted Schottky diodes previously used for ultra-high frequency applications [1]. Although several technologies are available for building THz sources and detectors, such as quantum cascade lasers (QCL), heterostructure barrier varactors (HBV) or hot electron bolometers (HEB), presently the Schottky technology is the most widespread used, including applications as frequency multipliers from several tens of GHz to few THz. The good performance of the PSBD-based circuits at room temperature have allowed to implement this technology in ground base and space-borne radio astronomy applications such as the Herschel Space Observatory [1], [2] and the ALMA observatory [3], [4]. Recently, we are carrying an intense research related to the Submillimeter Wavelength Instrument (SWI) proposed by the Spatial European Agency (ESA) in the frame of the future Jupiter ICe moons Explorer (JUICE) mission, working in two frequency channels: 540-640 GHz [5] and 1080-1280 GHz [6]. For the development of such ultra-high frequency multipliers it is necessary to have a precise description of the experimental values of the capacitance and resistance of the ultra-scaled GaAs PSBDs that are the core of the circuits. Indeed, excellent output power levels have been obtained during the last years by using fitted equations for the experimental C-V and I-V characteristics of the PSBDs [7], [8]. But such data are not often available, so that analytical models for the electrical characteristics of SBDs are typically used. The problem is that when reducing the size of the diodes for increasing the frequency of operation, the emergence of non-ideal phenomena can affect the accuracy of the models used in the circuit design process and thus dramatically reduce the final efficiency of the multiplication stage [4], [9], [10]. The advanced physical models used at JPL (including not only fringing capacitances in the equivalent circuit of the PSBDs, but also carrier inertia, influence on the resistance of the doping-dependent mobility, etc., as explained in [6] and [11]) have allowed to reach output frequencies of 1.5 THz [4]. But just the use of the simple model for the edge capacitances proposed by Louhi *et al.* in [9], jointly with an adequate modification of the value of the series resistance of the diodes (which has to be artificially increased), has allowed the increase of the output frequency of frequency multipliers up to 2.48-2.75 THz [12]. However, none of these models can accurately predict the output power of the circuits, and a good agreement between simulations and measurements can only be obtained if the models are adjusted once the experimental results are available. Therefore, the key point for the correct operation of the fabricated circuits is the experience of the designer in adequately tuning the values of the electrical parameters used in the models of the PSBDs. Since the most important

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parameter for optimizing the performance of frequency multipliers is the non-linearity of the C-V characteristic of the diodes, we will reassess the validity of the capacitance models used in the design of such applications, which are critical mainly when aiming at high-efficiency or high-power circuits at frequencies of the pump signal above 100 GHz. Also the I-V curve of the devices have to be correctly modeled, but this point is out of the scope of this paper.

We have to stress that the lumped-element circuit (LEC) model is valid in a certain the frequency range, since, even if using correct values for the capacitances and resistances of the PSBDs, such model fails when increasing the input frequency. For this sake, we refer to the results shown in [13], where a review of the available models for the design and optimization of Schottky diode based multipliers is made. Pardo *et al.*, using an harmonic balance circuit solver coupled to a lumped-element circuit representation of the diode (LEC-HB), compare the results provided by drift-diffusion and hydrodynamic transport models with those obtained with a one-dimensional Monte Carlo (MC) simulator (also coupled with the HB solver, MC-HB). The MC simulator is considered as a reference when comparing the different models of Schottky diodes, since, by accounting for all the microscopic phenomena taking place within the devices, it provides a precise description of the semiclassical electron transport even under large signal or high frequency excitations. The main conclusion extracted in [13] is that the operation of Schottky-diode based circuits up to very high frequencies (even above 1 THz) can be correctly described by means of simplified analytical LEC-HB simulators as long as correct values for the resistances and capacitances are used, which can be provided by means of MC simulations.

However, this conclusion is only valid as long as velocity saturation and carrier inertia phenomena are absent, i.e., at frequencies below a certain limit. Fortunately, the effect of velocity saturation can be avoided in experimental applications by reducing the bias and increasing the epilayer doping [14], thus allowing the LEC models to be valid for well-designed diodes at input frequencies even above 600 GHz (i.e. triplers approaching output frequencies of 2 THz). This result has been confirmed by dynamic simulations of the GaAs PSBDs studied in this work, carried out with our 2D-MC code, in which the influence of velocity saturation phenomena is not significant at input frequencies below 300 GHz. Above this limit, physical models accounting for these phenomena are necessary, as discussed in [11].

In this context, the aim of the present work is to calculate, by means of MC simulations, the static capacitance of GaAs PSBDs to be used in the design of THz circuits using LEC-HB models, and also analyze the microscopic origin of the fringing capacitance. To this end we will use the 2D-MC simulator presented in [15], [16]. From the calculated values of the capacitance we propose a simple compact analytical model for the C-V dependence, accounting for the influence of the surface charges on edge effects (EEs), which correctly describes the obtained results and can be readily included in commercial non-linear HB simulators. This analysis is especially important for high frequency applications, where the anode surface needs to be drastically reduced as the frequency increases and the available power is low, so that a precise design for an improved efficiency is highly demanded. The so-called "edge-effect" becomes important for such small PSBDs and can strongly modify the optimal conversion efficiency point. Previous studies of the EE have been performed by different authors [17], [18], but always considering an ideal epilayer-dielectric interface in the proximities of the Schottky contact, i.e. disregarding the depletion region present at the semiconductor surface originated by trapped charges. The aim of this work is to shed light on the microscopic origin of the EE in the capacitance of PSBDs, including the contribution of surface charges. The influence of the epilayer structure and the surface charges at the semiconductor-dielectric interface on the EE capacitance will be quantified in order to provide a compact model that can be easily implemented in design automation software such as ADS, which will allow the precise design of THz MMICs based on GaAs PSBDs.

The paper has been structured as follows. In Section II the physical simulator based on the 2D MC method and the geometry of the PSBDs are introduced. In Section III the analytical model to characterize the charge variations in Schottky diodes derived from MC results is presented, as well as the influence of the surface potential on the depletion region generated by the Schottky contact. A geometrical analysis is also carried out in this section to identify the physical origin of the observed charge variations and associated capacitance. Our main conclusions are finally drawn in Section IV.

II. Physical Model

A. Monte Carlo Simulator

The present study has been performed by using a semi-classical ensemble MC simulator of carrier transport self-consistently coupled with a 2D Poisson solver. Three non-parabolic spherical valleys (Γ, L, X) are used to model the conduction band of the GaAs semiconductor layers [19]. Ionized impurity, alloy, polar and nonpolar optical phonon, acoustic phonon and intervalley scattering mechanisms are taken into account, allowing the consideration of hot carrier effects in the proximities of flat-band in Schottky contacts [20]. Fermi-Dirac statistics, using a self-consistent calculation of the Fermi level, are imposed for the occupancy of energy states by means of the rejection technique when selecting the final state after scattering events [16]. This technique has already been successfully applied for the study of HEMTs [21]-[23]. Regarding the contact models, both the Schottky and the ohmic contacts are simulated as in [16], [20]-[23]. The Schottky contact is simulated as a perfect absorbing boundary, that is, all the carriers reaching the metal contact leave the structure and no carriers are injected from the metal into the semiconductor. This consideration leads to the modification of the Maxwellian velocity distribution of the electrons at some tens of nm from the Schottky interface to a perfect hemi-Maxwellian distribution at the interface [24]-[26]. Regarding the ohmic contact model, it imposes charge neutrality in the proximities of the electrode by injecting carriers with the appropriate thermal distribution (velocity-weighted hemi-maxwellian) at the lattice temperature [20].

In this work we focus on the determination of the junction capacitance as a function of the applied voltage (in reverse and forward bias below flat-band conditions) in 2D PSBDs. The junction capacitance in Schottky diodes is associated to bias-induced variations of the depletion region generated by the built-in voltage of the junction and the applied voltage. Additional (bias independent) depletion regions originated by the presence of surface charges at the semiconductor-dielectric interfaces can overlap the previous one, thus affecting the value of the junction capacitance. Such surface charges are accounted for in the simulator by means of the model used in [15], in which the value of the considered surface charge, σ, is related to that of a surface potential, V_S, by:

$$\sigma = -\sqrt{2qN_D|V_S|\varepsilon_{SC}}\ , \qquad (1)$$

where N_D is the semiconductor doping, ε_{SC} is the permittivity of the semiconductor and q is the electron charge. A frequent criterion to choose the V_S value considers that it is the surface potential necessary to bring the Fermi level of the semiconductor near the middle of the bandgap [16]. We will study the influence of the surface charges by simulating different Fermi-level pinning conditions, with values of V_S ranging from 0 V to a maximum of -0.7 V, the half of the GaAs band gap.

To compute the DC capacitance of the PSBDs, we monitor the average number of electrons present inside the diode at every bias point. The intrinsic capacitance is then calculated from the charge variation from point to point as $\Delta Q/\Delta V$, neglecting the dielectric capacitance between contacts, whose value is much smaller, and the parasitic contributions of the accesses.

B. Simulated Structure

The MC simulated structures are based in real PSBDs fabricated using the E-beam photolithography LERMA-LPN process, presented in [27], [28]. Fig. 1(a) shows an image of a real PSBD used in a frequency doubler at 280 GHz, which is part of the local oscillator chain of the 600 GHz frequency receiver presented in [5]. The red line indicates the transversal plane where the 2D MC simulated structure has been defined. Taking advantage of the symmetry of the anode, only half of the diode is considered in the simulation domain for reducing the computational requirements. The scheme of the simulated PSBDs is represented in Fig. 1(b), where the characteristic lengths are indicated. The GaAs layer structure consists of a highly doped n^+ substrate (with doping N_S) and a n epilayer (with low doping N_E). The Schottky contact is placed on the top of the epilayer, while the ohmic contact is deposited on the semiconductor substrate and isolated from the epilayer by etching and dielectric deposition (Si_3N_4), which also passivates the global structure. The simulated surface charges σ are placed at the epilayer-dielectric and substrate-dielectric interfaces [in red in Fig. 1(b)] and their value (for a given V_S) is calculated following (1), according to the doping level of each semiconductor layer.

The simulated geometry resembles as closely as possible the fabricated PSBD. The substrate thickness W_{Sub} and the ohmic contact length L_{OhmL} are large enough to ensure a flat potential profile at the bottom of the structure. The length of the dielectric region L_{Diel} that isolates the ohmic contact from the epilayer is similar to the epilayer thickness W_{EP}, determined by the technological process [29], [30].

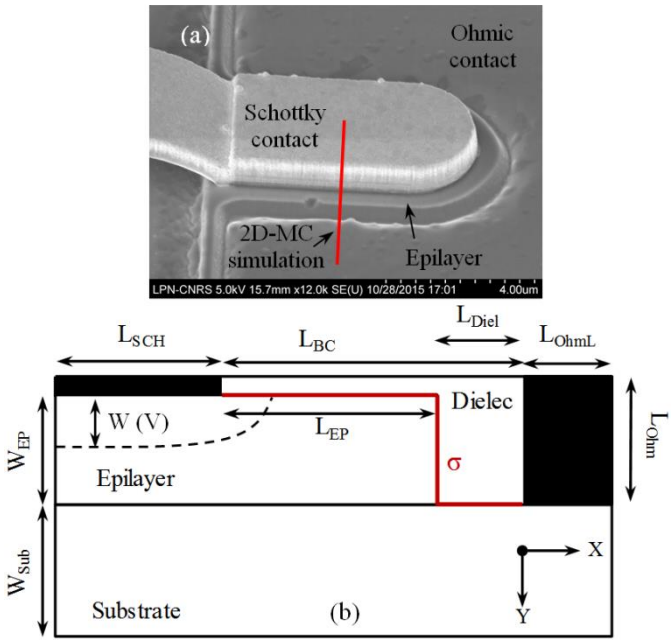

Fig. 1. (a) Image of a real PSBD fabricated by LERMA-LPN-CNRS and (b) scheme of the MC simulation domain based in the real devices.

Table I. Physical and geometrical parameters of the two simulated PSBDs.

Symbol	DiodeA	DiodeB
L_{SCH} (nm)	200	1500
W_{EP} (nm)	180	350
L_{EP} (nm)	230	460
L_{Diel} (nm)	120	240
L_{BC} (nm)	350	700
W_{Subs} (nm)	350	500
L_{OhmL} (nm)	300	500
N_E (cm^{-3})	$3\cdot10^{17}$	$1\cdot10^{17}$
N_S (cm^{-3})	$5\cdot10^{18}$	$5\cdot10^{18}$
V_B (V)	0.745	0.695

The simulated Schottky anode length L_{SCH}, and the epilayer length between contacts L_{EP}, thickness W_{EP} and doping level N_E will be modified to study the influence of the epilayer geometry on the depletion region generated by the Schottky contact. Since this work is focused on the study of the backward junction capacitance of the PSBD, which is especially important in multiplying applications, the epilayer thickness in the simulated structures will be always large enough to avoid the penetration of the depletion region into the substrate layer in the applied bias range [31].

According to these considerations, two different structures, presented in Table I, have been defined to carry out the study. The DiodeA structure is based on a PSBD used in the frequency mixer presented in [5] but with a thicker epilayer to allow for higher reverse biasing, while the DiodeB structure is based on the frequency doubler of the same receiver. These structures present a very different Schottky anode size L_{SCH} and a different epilayer doping level N_E. The

lengths L_{OhmL} and W_{Subs} are sufficiently large to avoid any artificial resistance coming from the simulation of the ohmic contact or the substrate. The geometry of the epilayer (W_{EP}, L_{EP}) is defined according to its doping level to ensure that the depletion region does not reach the substrate layer or the vertical epilayer-dielectric interface placed at a distance L_{EP} from the edge of the anode. Initially, a value of -0.5 V is considered for the surface potential V_S; then it will be modified in order to analyze its influence on the PSBD capacitance.

III. Results

From the integration of the number of particles inside the diode obtained with the MC simulation for each bias point, we evaluate the variation with the bias of the total charge in the structure (and hence the capacitance), which can be associated to the variation of the depletion region generated by the Schottky contact. The charge variation has been analyzed in bias steps of 0.5 V when strongly reverse biasing the diode and 0.05 V when near flat band conditions. The *C-V* characteristics of nanometer scale GaAs PSBDs with realistic geometries (as shown in Table I) will then be obtained.

The simulations are also able to show the local contribution of the different regions of the device to the charge variation (and to the total capacitance of the diode) by subtracting the electron concentration in each cell of the mesh structure at two different bias points, as shown in Fig. 2. As clearly observed in the figure, the intrinsic capacitance of PSBDs deviates from the ideal value of a parallel-plate capacitor due to the presence of a depletion region not only below the anode but also around its edge. Moreover, the variations of the bias induced depletion region (and therefore the total junction capacitance) become strongly affected by the presence of surface charges when these are considered in the simulations, Figs. 2(b) and (d), mainly because of a decreased contribution of EEs.

The results of the 2D-MC model for the depleted charge (per unit length in the non-simulated dimension, thus in C/m) will be compared with the ideal value of the charge in the depletion region generated by the Schottky contact in the absence of EEs [32]:

$$Q_{Ideal}(V) = -L_{SCH} q N_E W(V) = -L_{SCH}\sqrt{2q\varepsilon_{sc}N_E(V_B - V)}\ , \qquad (2)$$

where V_B is the built-in voltage of the Schottky contact, V the applied bias and

$$W(V) = \sqrt{\frac{2\varepsilon_{sc}(V_B - V)}{qN_E}} \qquad (3)$$

the depth of the depletion region. In the MC simulation, the charge depleted by the bias voltage Q_{MC} is calculated as the difference between the total charge in the diode for a given bias and that present under flatband conditions.

The dependence of the depleted charge on the bias (below flatband) obtained with the 2D-MC simulations of DiodeA and DiodeB, normalized to the simulated anode length, is plotted in Fig. 3(a) when a surface potential V_S=-0.5 V is considered. While in both diodes the expected $\sqrt{(V_B - V)}$ dependence of the depleted charge is followed, there is a discrepancy when comparing the MC results with the ideal charge variation given by (2). A larger difference is observed for DiodeA, mainly because it has a smaller size (lower L_{SCH}). However, if the ideal depleted charge given by (2) is subtracted from the MC results, and we remove the normalization by the length L_{SCH}, the resulting difference is practically the same for both diodes, as plotted in Fig. 3(b). Fig. 3(b) also shows that the additional depleted charge due to the EE presents a linear dependence on the bias (in reverse bias, far from flatband conditions), in good agreement with previous predictions [17], [18].

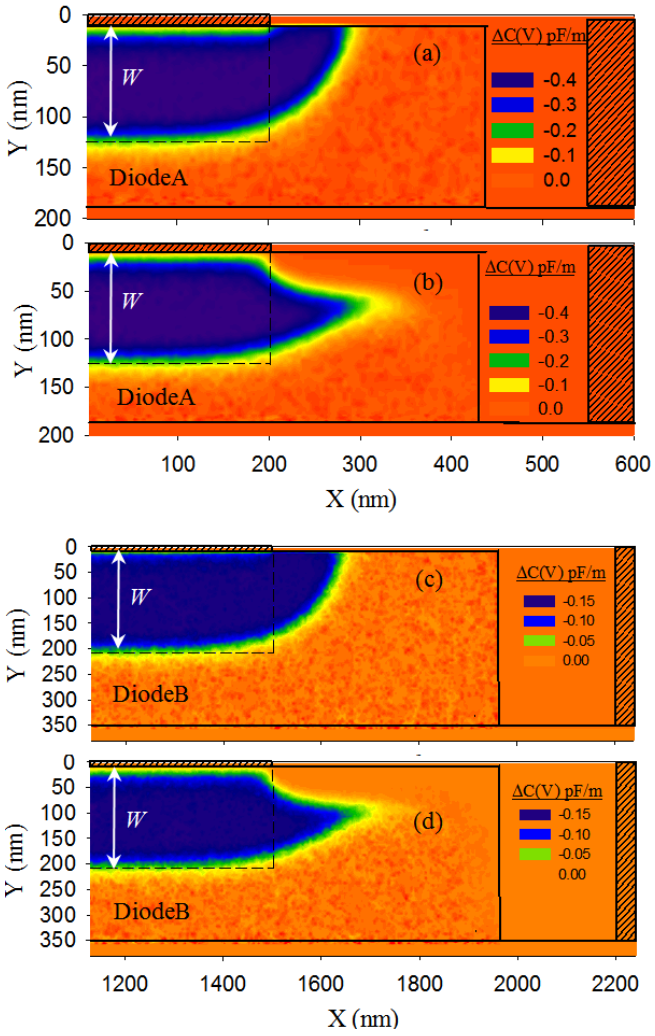

Fig. 2. Map of the local contribution to the total capacitance per unit length (calculated as the variation of the charge per unit length between the bias points V=V_B and V =-2.0 V, divided by the voltage difference) for both (a) and (b) DiodeA and (c) and (d) DiodeB. The MC simulations are performed considering (a) and (c) a null surface potential and (b) and (d) V_S=-0.5 V. The depth of the depletion region calculated within the total depletion assumption, W, is shown, and the rectangular shaded region indicates the depletion region expected for an ideal parallel-plate capacitor. Note that the axes have been scaled between DiodeA and DiodeB due to the different size of the diodes.

This result indicates that the additional charge contribution originated from the 2D geometry of the diodes (EE) is independent of the anode size and doping level of the

epilayer, result already obtained in analytical calculations of the electric potential distribution in metal-semiconductor junctions [33], [34]. Indeed, we have performed simulations in a large variety of diodes and all of them follow this universal behavior. However, it is important to remark that the description of the response of PSBDs at very high frequencies (above the range of validity of the standard LEC approach) requires more than a single capacitance to account for complex non-harmonic effects related to velocity saturation, which do depend on the doping level of the epilayer [13].

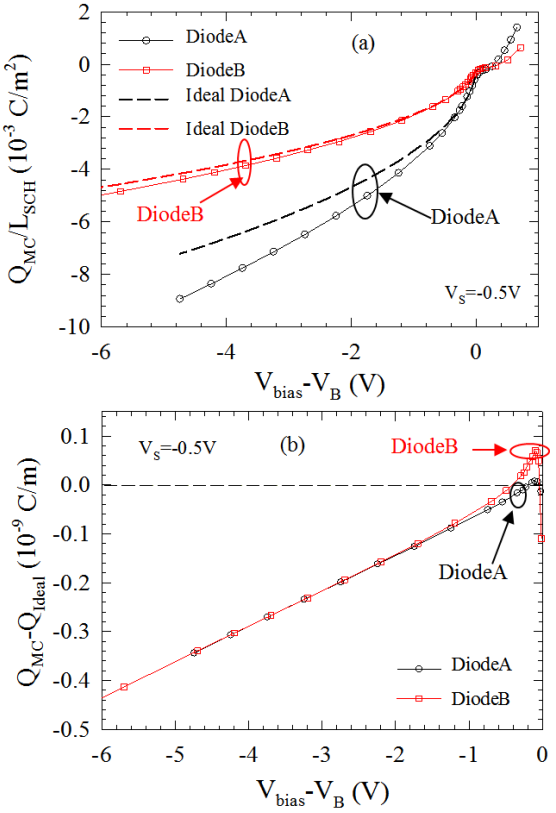

Fig. 3. (a) Depleted charge per unit surface, obtained by normalizing by L_{SCH} the charge per unit length obtained with 2D-MC simulations, compared with the ideal one (dashed lines) for DiodeA and DiodeB. (b) Excess charge per unit length depleted at the edges of the Schottky contact due to 2D phenomena calculated by subtracting the ideal charge given by eq. (2) from the 2D-MC result. A surface potential V_S=-0.5 V has been considered in these simulations.

As observed in Fig. 2, this 2D EE observed with our MC model is strongly dependent on the presence or not of surface charges at the semiconductor-dielectric interface. We can therefore analyze the influence of the surface potential of the epilayer on the additional depleted charges associated to the 2D effects by plotting, Fig. 4, the difference between the MC results and the ideal depleted charge (Q_{MC}-Q_{Ideal}) for different values of V_S. As observed, it is possible to conclude that the linear tendency remains for any surface potential considered in the simulation, but with a slope that slightly depends on V_S.

According to the previous observations, and in agreement with the classical models [17], [18], we can propose a modification of (2) able to account for the 2D effects appearing in PSBDs by including an additional linear term, and considering a dependence of the EE parameter on the surface potential.

$$Q(V) = -L_{SCH}\sqrt{2\varepsilon_{sc}qN_E(V_B - V)} + \beta(V_S)\varepsilon_{sc}(V - V_B), \quad (4)$$

where $\beta(V_S)\cdot\varepsilon_{sc}$ is the slope of the representation of Q_{MC}-Q_{Ideal} vs. V-V_B [Figs. 3(b) and (4)] with $\beta(V_S)$ the dimensionless EE parameter. This parameter was already defined in [17], [18] as a phenomenological way of characterizing EEs in PSBDs, but it was taken as an universal constant. In fact, Eq. (4) highlights that the EEs do not depend neither on the anode size nor on the doping level of the epilayer. However, our MC simulations clearly show that the value of the EE parameter can be affected by the presence surface charges at the epilayer-dielectric interface.

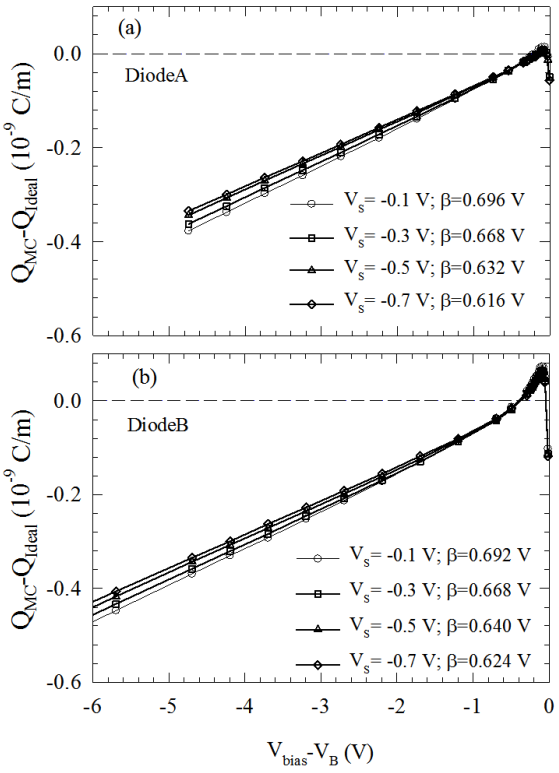

Fig. 4. Charge per unit length depleted by the Schottky contact in excess of the ideal value given by eq. (2) (Q_{MC}-Q_{Ideal}) for (a) DiodeA and (b) Diode B when considering V_S= -0.1, -0.3, -0.5 and -0.7 V.

From the fitting of the MC results with (4) we have extracted the dependence of β on V_S and plotted it in Fig. 5 for both simulated diodes. We can observe that, in spite of the differences in the geometry and doping levels, DiodeA and DiodeB show very similar values of the EE parameter. This result is coherent with the classic model firstly proposed in [17] and extended in [18], in which a parameter called D_1 is proposed for characterizing the EE, with an universal value of 0.36, which coincides with our calculations in the absence of surface charges (since $\beta_0 \equiv 2D_1$=0.72). The decrease of $\beta(V_S)$ with increasing negative values of V_S observed in Fig. 5 is connected with the lower charge variations at the edge of the Schottky contact due to the depletion induced by the surface charges at the semiconductor-dielectric interfaces, as clearly illustrated in Figs. 2(b) and (d).

We can then propose a second order polynomial approximation for $\beta(V_S)$ that can be considered to be

universal according to the MC results, since it is independent of the properties of the semiconductor beneath the contact, and so is the edge capacitance (as we will show next):

$$\beta(V_S) = 0.720 + 0.216 \cdot V_S + 0.105 \cdot V_S^2 \ , \qquad (5)$$

where $V_S<0$ is defined in *Volts*.

Starting from the analytical expression for $Q(V)$, given in (4), we can straightforwardly extend our analysis to the behavior of 2D EE in the capacitance of PSBDs, and provide a simple analytical expression to obtain the value of the capacitance per unit length of the PSBDs, $C(V)$, as:

$$C(V) = \frac{dQ(V)}{dV} = L_{SCH}\frac{\varepsilon_{sc}}{W} + \beta(V_S)\varepsilon_{sc} = C_{Ideal}(V) + C_{EE} \ \text{(in } F/m\text{)}. \qquad (6)$$

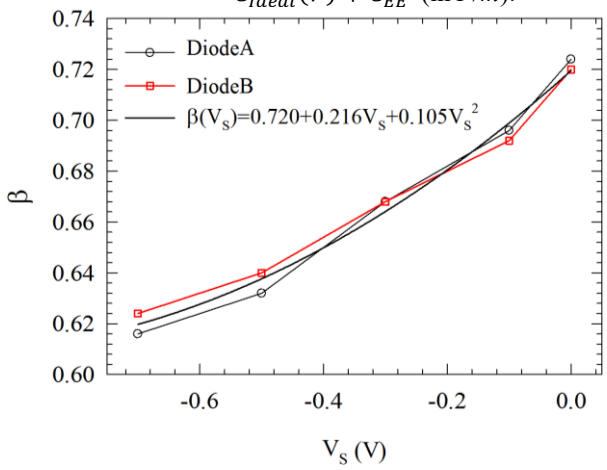

Fig. 5. EE parameter variation when considering a surface potential sweep from 0 V to -0.7 V for DiodeA and DiodeB. An analytical approximation of $\beta(V_S)$ in the considered range is included.

Eq. (6) reveals a deviation from the ideal parallel-plate capacitance, $C_{Ideal}(V)$, due to the presence of a constant contribution to the total capacitance of the PSBD, $C_{EE}=\beta(V_S)\varepsilon_{sc}$, originated by the 2D EEs, and whose value is only dependent on the dielectric constant of the semiconductor and the parameter $\beta(V_S)$.

In Fig. 6, the results of the MC simulations using three different values of V_S are compared with the analytical expression (6) [using the values of $\beta(V_S)$ provided by eq. (5)] and the ideal parallel-plate capacitance $C_{Ideal}(V)$. Due to the EE, $1/C^2$ is not a straight line anymore, but it is deviates from the ideal behavior. Such deviation is more pronounced in DiodeA as the anode size is reduced, since the ideal contribution decreases while the contribution of C_{EE} remains constant. The implementation of this capacitance model in a non-linear HB simulator and its usefulness with respect previous models is a matter of a different analysis, but the conclusion obtained in [18] has already been verified: the presence of EEs in small anodes leads to a more reactive impedance of the PSBD as the excited voltage signal enters in the inverse region, what leads to a reduction of the conversion efficiency of the multiplier as well as to a modification of the optimal bias.

In conclusion, (5) and (6) are able to correctly reproduce the results of the capacitance of PSBDs obtained with the MC simulations, so that they could even be used to extract the values of V_S from the measurements of the *C-V* curve of any kind of PSBDs. However, this analysis is extremely difficult, since the parasitic contributions to the intrinsic capacitance of the PSBD should first be deembedded. Indeed, for practical design purposes, EE and parasitic contributions could both be included in (6) just by modifying the value of β, so that this simple compact model for the PSBD capacitance can be easily implemented in commercial circuit simulators like ADS.

We must remark that our study of EEs has been performed with a 2D representation of a rectangular Schottky anode, assuming the diode is homogenous in the non-simulated dimension. This means that in a realistic case of a Schottky contact with a given geometry, to calculate the additional contribution of EEs to the absolute diode capacitance, C_{EE} should be multiplied by the total length of the diode contour.

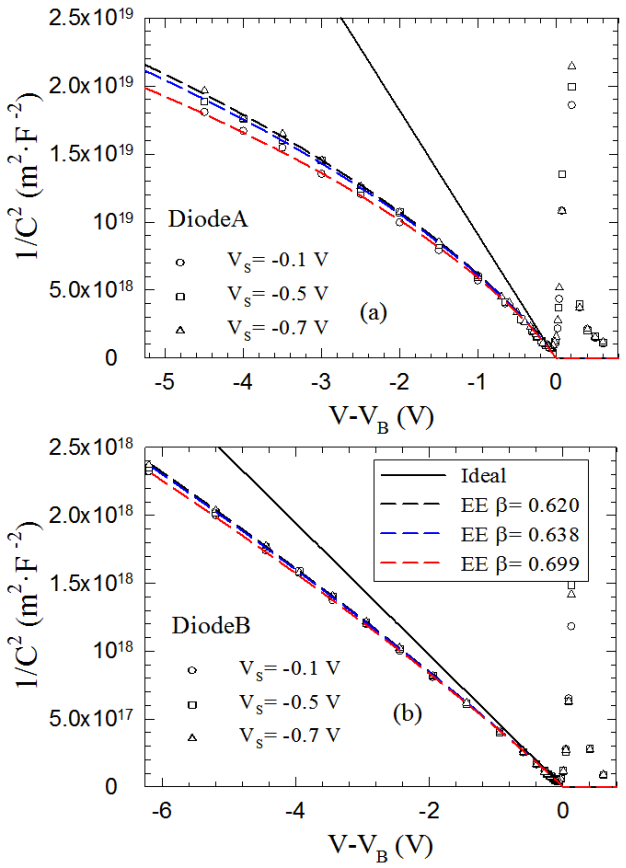

Fig. 6. Comparison between the values of $1/C^2$ in (a) DiodeA and (b) Diode B obtained with the MC simulations (symbols) and the analytical expression of eq. (6) (dashed lines) when considering V_S=-0.1, -0.5 and -0.7 V. The solid black line represents the ideal parallel-plate capacitance of Schottky diodes.

Additionally, in the case of circular anodes a further correction to the value of the capacitance is necessary to account for the circular shape of the EE depletion region, consisting in a new term in (6) which involves a second EE parameter, D_2 [18]. The value of D_2 (0.34 if no surface effect is considered) has in turn to be modified also by the effect of V_S in a factor $[\beta(V_S)/\beta_0]^2$ (the square exponent appears when integrating (6) in a circular geometry).

As a result, extending the model proposed in [18] to the case of a general shape and considering surface effects, the absolute capacitance of a PSBD can be calculated as:

$$C_T(V) = A\frac{\varepsilon_{sc}}{W(V)} + L_{Contour}2D_1\frac{\beta(V_S)}{\beta_0}\varepsilon_{sc} + 3D_2\left[\frac{\beta(V_S)}{\beta_0}\right]^2\varepsilon_{sc}W(V) \quad (\text{in } F), \qquad (7)$$

$$\text{with } \frac{\beta(V_S)}{\beta_0} = 1 + 0.300\cdot V_S + 0.146\cdot V_S^2$$

which is the result of the addition of the ideal parallel-plate term (proportional to the area of the anode, *A*), the EE term (proportional to the length of the contour of the anode, $L_{Contour}$, and independent of the epilayer doping) and a third term associated to the circular sections of the EE depletion region (independent of the anode geometry but dependent on the biasing and epilayer doping, as it is proportional to *W*). Notice that circular sectors are not only present in the depletion region of circular anodes, but also at the corners of rectangular ones, and their contribution to the total capacitance is not accounted for by the first two terms in (7). Therefore, the third term must be included even in the case of rectangular geometries. Indeed, such a term does not contain any dependence on characteristic parameters of a circular geometry. The third contribution to the capacitance is not present in our MC simulations, since the 2D approach implies homogeneity in the non-simulated dimension, and therefore absence of any circular section in the EE depletion region in such a direction.

IV. Conclusions

By means of 2D MC simulations of PSBDs, we have analyzed the deviations of the internal charge variation and the associate intrinsic capacitance with respect to the ideal 1D behavior. The 2D shape of the depletion region beneath the Schottky anode leads to an excess of depleted charge (EE) which increases linearly with respect to the reverse applied voltage, thus contributing with a constant term to the global capacitance of the PSBD (characterized by an EE parameter, β), which is proportional to the length of the contour of the anode but independent of the doping level of the epilayer. By modeling the surface charges at the epilayer-dielectric interface (characterized by the value of its surface potential V_S), we have evidenced a dependency of β on V_S, leading to a reduction up to a 15% from its nominal value β_0 (with a dependence that can be approximated by a second order polynomial equation). The compact model provided by the analytical eqs. (5) and (7) can be easily implemented in LEC-HB simulators (with correct values of the series resistance obtained with a 2D current model) for an accurate prediction of the diode response in multiplying applications up to, at least, 300 GHz LO input signal [18].

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